AVANTEK
MILPITAS

TECHNICAL MANUAL
FOR
ERROR RATE TEST SET
MODEL 271B

SERIAL NUMBER _____

Bowmar
WHEN QUALITY COUNTS

Communications Test Equipment

Bowmar/ALI Inc.
531 Main Street
Acton, Mass. 01720

TECHNICAL MANUAL
FOR
ERROR RATE TEST SET
MODEL 271B

SERIAL NUMBER _____

BOWMAR/ALI, INC.
531 Main Street
Acton, Massachusetts 01720

Rev. L
October, 1984

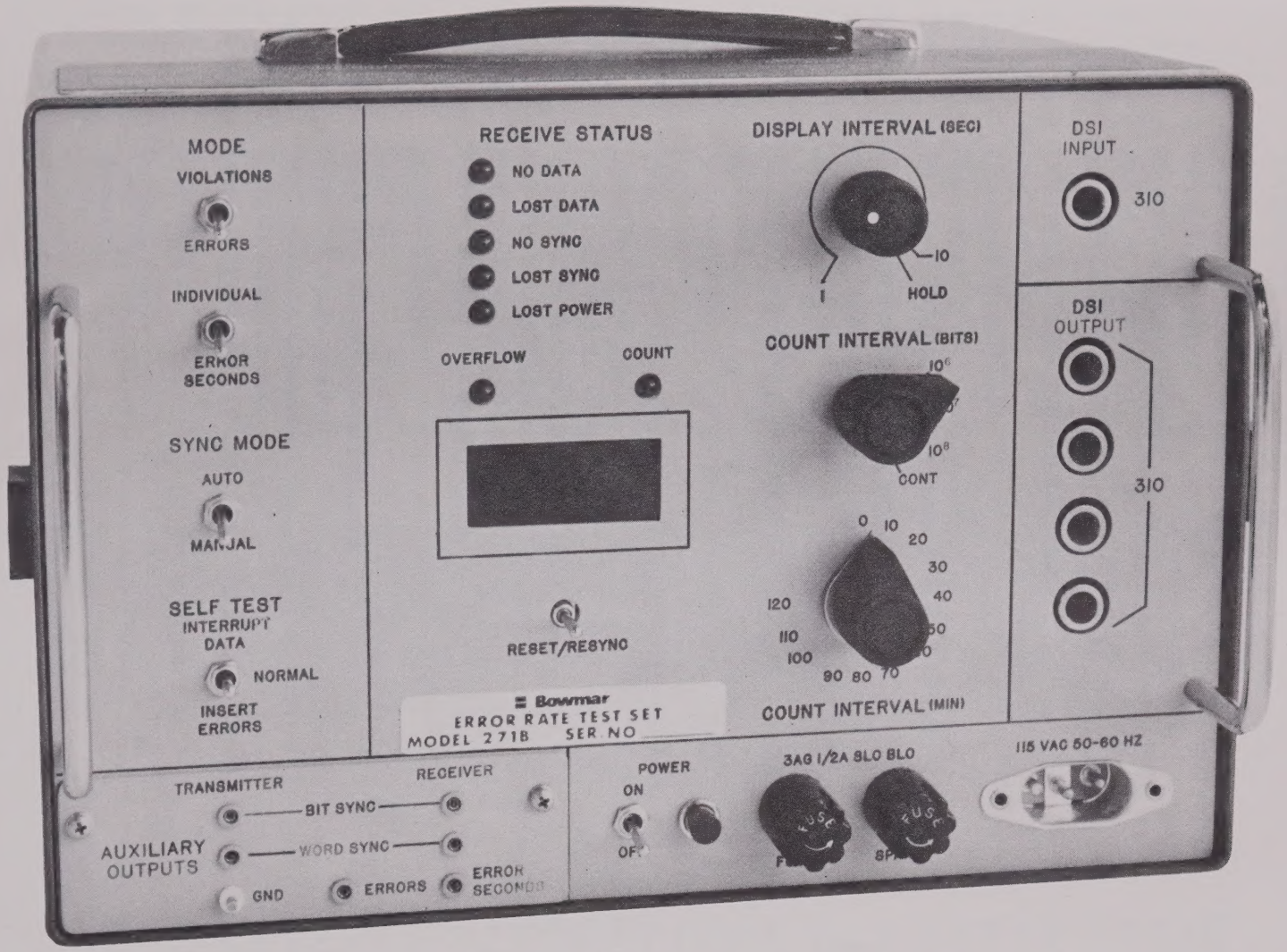
SPECIAL NOTICE

Bowmar/ALI, Incorporated

Proprietary Information

WARNING - Do not copy or distribute.

This technical manual contains proprietary information of Bowmar/ALI, Incorporated and its receipt or possession does not convey any rights to reproduce, disclose its contents, or to manufacture, use or sell in whole or in part anything it may describe. Reproduction, disclosure, or use without the specific written authorization of Bowmar/ALI, Incorporated is strictly forbidden. This restriction does not limit the right to use information contained in this Manual if it has been validly obtained from another source or has been placed in the public domain without the fault of any person, firm or corporation in possession of this manual.



ERROR RATE TEST SET

TABLE OF CONTENTS

		Page
1.0	INTRODUCTION	1-1
1.1	Equipment Description	1-1
1.2	Scope of Manual	1-1
1.3	Specification Summary	1-1
2.0	INSTALLATION INSTRUCTIONS	2-1
2.1	Preparation	2-1
2.2	Checkout/Self Test	2-1
2.3	Operation	2-4
2.4	Printer/Computer Interface (271B-2 Only)	2-4
3.0	OPERATION AND APPLICATIONS	3-1
3.1	Controls, Indicators, and Jacks	3-1
3.2	Applications	3-6
4.0	THEORY OF OPERATION	4-1
4.1	General	4-1
4.2	Transmitter	4-1
4.3	Receiver	4-2
4.4	Transmitter Circuits (A5 Module)	4-6
4.5	Receiver Circuits	4-11
4.5.1	Receiver Module (A4)	4-11
4.5.2	Receiver Reference Module (A1)	4-14
4.5.3	Receiver Logic Module (A2)	4-18
4.5.4	Display Module (A8)	4-20
4.6	Power Supply Assembly (A6)	4-21
5.0	MAINTENANCE	5-1
5.1	General	5-1
5.2	Test Equipment Requirements	5-1
5.3	Calibration Procedure	5-1
5.4	Performance Checks	5-8
5.4.1	Transmitter Checks	5-8
5.4.2	Receiver Checks	5-13
6.0	DRAWINGS	6-1
7.0	PARTS LIST	7-1
7.1	General	7-1

1.0 INTRODUCTION

1.1 Equipment Description

The Error Rate Test Set is a lightweight, portable instrument capable of reliably checking T1 lines, T1 to T2 (M12) multiplexers, T1 to microwave modems, and similar digital transmission equipment. Checks are achieved by injecting a repeating pattern of data bits from the Test Set's transmitter section to a system under test, then monitoring the system's output with a receiver section from the same or a second Test Set. The receiver section may be set to detect either logical errors or bipolar violations, and it may also be set to tally the errors or violations individually or by blocks over a preselected interval of time. The resultant count is then furnished for visual access on the Test Set's digital display.

The 271B-2 Error Rate Test Set is equipped with a printer/computer interface. This interface is TTL compatible and provides all the signals necessary to implement remote readout, remote printout, and/or remote control of the Test Set. A complete description of these features is located in Section 2.4. It should be noted that this interface is provided on the 271B-2 Test Set only.

The Error Rate Test Set is protected by an outer housing which has been designed for durability as well as portability. A carrying handle is fitted to the top of the unit, and a cover which matches the housing protects the front panel. The power cord may be stored inside the cover. The front panel is fitted with a protective handle on each side. Controls, indicators, etc. are well delineated and labelled for quick access.

1.2 Scope of Manual

This manual contains descriptive detail of the Error Rate Test Set plus related applications notes, maintenance information, diagrams, and parts information. Descriptive detail is reduced to categories of physical and functional specifications, operating procedures, and operating principles. The manual's purpose is to provide sufficient familiarization to enable effective use and proper maintenance of the Test Set.

1.3 Specification Summary

Output Pattern:	A 1,048,575 bit quasi-random pattern limited to 14 consecutive zeros; compatible with Western Electric J98710R Quasi-Random Signal Source.

Input: Balanced; one jack which accepts a WE 310-type plug (T & R).

Outputs:

A. Main: balanced; four jacks which accept WE 310-type plugs (T & R).

B. Auxiliary: unbalanced; six pin jacks which allow monitoring of the signals listed below, plus a ground (GND).
   1. TRANSMITTER BIT SYNC
   2. RECEIVER BIT SYNC
   3. TRANSMITTER WORD SYNC
   4. RECEIVER WORD SYNC
   5. ERRORS
   6. ERROR-SECONDS

Controls

MODE Switches:
- 2-position: 1. VIOLATIONS, 2. ERRORS
- 2-position: 1. INDIVIDUAL, 2. ERROR-SECONDS

SELF TEST Switch:
- 3-position: 1. INTERRUPT DATA (momentary), 2. NORMAL, 3. INSERT ERRORS (momentary)

SYNC MODE Switch:
- 2-position: 1. AUTO, 2. MANUAL

DISPLAY INTERVAL (SEC) Control: 1 to 10 seconds, plus a detent setting for HOLD.

COUNT INTERVAL (BITS) Switch:
- 5-position: 1. 10^6, 2. 10^7, 3. 10^8, 4. CONT, 5. Timer

COUNT INTERVAL (MIN) Timer: 0 to 2 hours; mechanical.

POWER Switch:
- 2-position: 1. ON, 2. OFF

RESET/RESYNC Switch: Momentary toggle.

Indicators

Display:	3-digit; solid state.
RECEIVE STATUS Indicators:	5 separate indicators; solid state: 1. NO DATA 2. LOST DATA 3. NO SYNC 4. LOST SYNC 5. LOST POWER
Display Status Indicators:	2 separate indicators; solid state: 1. COUNT 2. OVERFLOW
POWER Indicator:	1 neon lamp to show power-on condition.
Fuses:	2 fuses (1 spare); 3 AG, 1/2 A, slow blow.
Power:	115 V ac ±10%, 50 to 60 Hz, single phase.
Receiver Input Threshold:	0.2 to 5.0 V peak.
Sync. Acquisition Time:	Less than 200 clock pulses. (Test Set will not resync on isolated error bursts of less than 6 consecutive errors.)

Transmitter Output
Bipolar Pulse Characteristics

Height of output pulse:	3 ± 0.3 V into 100 Ω load.
Unbalance in height of negative and positive pulse:	0.15 V
Width of output pulse (half amplitude):	324 ± 30 nsec
Unbalance in width of negative and positive pulse:	± 15 nsec
Maximum rise or fall time:	80 nsec
Overshoot at trailing edge of pulse:	10 to 30% of pulse height with decay to 10% or less of base line-to-peak value within 400 nsec.

Auxiliary Outputs

All Outputs:	A. Amplitude: unbalanced, nominal +5 volts switched to ground for duration of pulse. B. Source Impedance: less than 100 Ω.
TRANSMITTER BIT SYNC and RECEIVER BIT SYNC:	Square wave; 1.544 MHz Transmitter and Receiver Clock.
TRANSMITTER WORD SYNC and RECEIVER WORD SYNC:	340 nsec pulse; occurs once every 1,048,575 bits.
ERRORS:	340 nsec pulse; occurs once for every detected error.
ERROR-SECONDS:	500 ± 25 msec pulse; occurs once every block if one or more errors are detected. * * This output is not affected by operation of either the DISPLAY INTERVAL or COUNT INTERVAL controls.
Initial Oscillator Frequency:	1.544 MHz ± 30 Hz with Test Set operating temperature of 0° to 50° C.
Operating Environment:	0° to 50° C (32° to 120° F); to 95% relative humidity.
Dimensions:	8-1/4" D x 9-5/8" H x 12-1/8" W.
Weight:	13-1/2 pounds, 271B; 14 pounds, 271B-2.

2.0 INSTALLATION INSTRUCTIONS

2.1 Preparation

a. Remove the Error Rate Test Set from its shipping container.

b. Remove the front cover.

c. Check for the presence of 3AG, 1/2 A, slow blow fuses.

d. Remove the power cord from the front cover and connect the Test Set to a 115 V ac, 50-60 Hz, single phase power source.

e. Set the POWER switch to ON and note whether or not the indicator illuminates.

2.2 Checkout/Self Test

Follow the procedure outlined below.

a. Set switches to the following initial positions:

MODE	
VIOLATIONS/ERRORS	- to VIOLATIONS
INDIVIDUAL/ERROR-SECONDS	- to INDIVIDUAL
SYNC MODE	- to MANUAL
SELF TEST	- to NORMAL
DISPLAY INTERVAL (SEC)	- to '1' (full counterclockwise)
COUNT INTERVAL (BITS)	- to '10^6'
COUNT INTERVAL (MIN)	- to '0'
RESET/RESYNC	- momentarily actuate and release

b. Observe indicators for the following initial responses:

NO DATA	- off
LOST DATA	- off
NO SYNC	- on
LOST SYNC	- on
LOST POWER	- off
OVERFLOW	- off
COUNT	- alternately on for approximately 2/3 second, off for approximately 1 second
Display	- '000'

/c. Turn the DISPLAY INTERVAL (SEC) control clockwise to the '10' position. The COUNT indicator should alternately be on for approximately 2/3 second and off for approximately 10 seconds.

/d. Place the DISPLAY INTERVAL (SEC) control in its HOLD (detent) position and momentarily operate the RESET/RESYNC switch. The COUNT indicator should come on for approximately 2/3 second and then remain off indefinitely. Check the off condition for at least twenty seconds.

e. Place the DISPLAY INTERVAL (SEC) control at some point between '1' and '5'. Hold the SELF TEST switch at its INSERT ERRORS position. The indicated count on the Display should change by increments of two from a starting count of '000' to a final count of '008' while the COUNT indicator is on. At the count of '008', the Display should hold for the period set by the DISPLAY INTERVAL (SEC) control, then it should clear to '000' and begin a new cycle. The first count interval may not yield a total of eight errors, but each succeeding interval should register a count of '008' on the Display.

f. Holding the SELF TEST switch at its INSERT ERRORS position, change the COUNT INTERVAL (BITS) switch from 10^6 to 10^7. The indicated count on the Display should perform as it did in Step e, however, a full count interval should now register '080' on the Display.

g. Holding the SELF TEST switch at its INSERT ERRORS position, change the COUNT INTERVAL (BITS) switch from 10^7 to 10^8. The indicated count on the Display should perform as it did in Steps e and f, however, a full count interval should now register '800' on the Display.

h. Holding the SELF TEST switch at its INSERT ERRORS position, change the COUNT INTERVAL (BITS) switch from 10^8 to CONT and momentarily operate the RESET/RESYNC switch. The count on the Display should accumulate as in the preceding steps, and the OVERFLOW indicator should come on as the Display goes from '998' to '000'.

i. Holding the SELF TEST switch at its INSERT ERRORS position, momentarily operate the RESET/RESYNC switch. As it is operated, the Display should clear to '000', and the OVERFLOW and COUNT indicators should go off; the COUNT indicator should come on again within 2/3 second of switch release.

j. Release the SELF TEST switch and return the COUNT INTERVAL (BITS) switch to its 10^6 position.

k. Reset the VIOLATIONS/ERRORS switch to ERRORS, and momentarily operate the RESET/RESYNC switch. The Display indication should be '000' and all RECEIVE STATUS indicators should be off.

l. Hold the SELF TEST switch at its INTERRUPT DATA position. The NO DATA and NO SYNC indicators should come on. The LOST DATA indicator may come on.

m. Release the SELF TEST switch. The NO DATA indicator should go off, the LOST DATA indicator should be on, and the NO SYNC indicator should remain on; at the same time, the Display should show '888' with an OVERFLOW indication during the count interval, and any number with OVERFLOW at the end of the count interval.

n. Momentarily operate the RESET/RESYNC switch. The NO DATA, LOST DATA, NO SYNC, and LOST SYNC indicators should be off, and the Display should read '000' with no OVERFLOW indication.

o. Set the SYNC MODE switch at AUTO, and hold the SELF TEST switch at INTERRUPT DATA. The NO DATA and NO SYNC indicators should come on. The LOST DATA and/or the LOST SYNC indicators may come on.

p. Release the SELF TEST switch. The NO DATA and NO SYNC indicators should go off and the LOST DATA and LOST SYNC indicators should be on. The Display should read '000'.

q. Momentarily operate the RESET/RESYNC switch. The LOST DATA and LOST SYNC indicators should go off.

r. Hold the SELF TEST switch at its INSERT ERRORS position. The COUNT indicator should come on, and the Display should change by increments of two to a final count of '008'. Then it should clear to '000' and begin a new cycle.

s. Reset the INDIVIDUAL/ERROR-SECONDS switch to ERROR-SECONDS. Set the COUNT INTERVAL (BITS) switch to CONT. Hold the SELF TEST switch at INSERT ERRORS and momentarily operate the RESET/RESYNC switch. The COUNT indicator should come on, and the Display should increment at a rate of approximately once per second.

t. Holding the SELF TEST switch at INSERT ERRORS, change the VIOLATIONS/ERRORS switch to VIOLATIONS. The COUNT indicator should be on, and the Display should continue to increment at the rate of approximately once per second.

u. Change the COUNT INTERVAL (BITS) switch to the Timer (down) position. The COUNT indicator should go off within 2/3 second, but the Display should not clear to '000'.

v. Set the COUNT INTERVAL (MIN) switch at some arbitrary position past '20', and momentarily operate the RESET/RESYNC switch. The Display should clear to '000' and the COUNT indicator should come on within 2/3 second. Hold the SELF TEST switch at INSERT ERRORS. The Display should increment at the once-per-second rate. Return the SELF TEST switch to NORMAL position. The Display should not increment. There will be considerable, but normal, delay between the operation of the SELF TEST switch and the reaction of the Display.

w. Manually return the COUNT INTERVAL (MIN) switch to its '0' position, at which point an audible click will be heard. The Timer may continue to tick for some time. The COUNT indicator should go off within 2/3 second of the Timer's click, but the Display should not clear.

x. Momentarily operate the POWER switch to the OFF position and back to the ON position. The LOST POWER indicator should come on and remain on. Other RECEIVE status indicators may also come on. Operating the RESET/RESYNC switch should extinguish the LOST POWER and LOST DATA indicators. Other indicators may remain on.

2.3 Operation

When Checkout is satisfactory, proceed with desired operations. Refer to the Instruction Plate on the top of the case for simplified operating procedures.

2.4 Printer/Computer Interface (271B-2 Only)

Listed in Table 2-1 are all of the signals appearing on the Interface Connector, their specific functions, and pertinent details of the interface circuitry within the Test Set itself. Further discussion of the signals and their electrical contraints is given in this section, along with complete instructions for remote control of the Test Set. External connection to the Printer/Computer Interface Connector is made by using an Amphenol No. 57-30500 (or equivalent) connector.

2.4.1 Remote Control

The Test Set may be placed under remote control by placing the front panel switches in their open-circuit positions and manipulating the control lines via the interface connector. The correct switch positions for remote control are listed in Table 2-2, and the functions of the control lines are listed in Table 2-1. All control lines, except Interrupt Data, pin 22, are TTL compatible and may be interfaced with TTL driver circuits.

Table 2-1: Printer/Computer Interface Connector - Signals and Pin Assignments (271B-2 only)

Pin No.	Signal ID	Signal Function	Interface
1	$10^0 - \overline{1}$	Units digit, BCD inverted, A bit	TTL output
2	$10^0 - \overline{2}$	Units digit, BCD inverted, B bit	TTL output
26	$10^0 - \overline{4}$	Units digit, BCD inverted, C bit	TTL output
27	$10^0 - \overline{8}$	Units digit, BCD inverted, D bit	TTL output
3	$10^1 - \overline{1}$	Tens digit, BCD inverted, A bit	TTL output
4	$10^1 - \overline{2}$	Tens digit, BCD inverted, B bit	TTL output
28	$10^1 - \overline{4}$	Tens digit, BCD inverted, C bit	TTL output
29	$10^1 - \overline{8}$	Tens digit, BCD inverted, D bit	TTL output
5	$10^2 - \overline{1}$	Hundreds digit, BCD inverted, A bit	TTL output
6	$10^2 - \overline{2}$	Hundreds digit, BCD inverted, B bit	TTL output
30	$10^2 - \overline{4}$	Hundreds digit, BCD inverted, C bit	TTL output
31	$10^2 - \overline{8}$	Hundreds digit, BCD inverted, D bit	TTL output
7	$\overline{\text{OVERFLOW}}$	Logical 0 when OVERFLOW indicator on	TTL output
8	$\overline{\text{COUNT}}$	Logical 0 when COUNT indicator on	TTL output
9	$\overline{\text{NO DATA}}$	Logical 0 when NO DATA indicator on	TTL output
10	$\overline{\text{LOST DATA}}$	Logical 0 when LOST DATA indicator on	TTL output
11	$\overline{\text{NO SYNC}}$	Logical 0 when NO SYNC indicator on	TTL output
12	$\overline{\text{LOST SYNC}}$	Logical 0 when LOST SYNC indicator on	TTL output
13	$\overline{\text{LOST POWER}}$	Logical 0 when LOST POWER indicator on	TTL output
15	RESET/RESYNC	Ground to reset Test Set	Switch, 11 TTL inputs, 1KΩ to +5V
16	VIOLATIONS/ERRORS	Ground or logical 0 for VIOLATIONS mode Open or logical 1 for ERRORS mode	Switch, 2 TTL inputs, 1KΩ to +5V
17	INDIVIDUAL/ ERROR-SECONDS	Open or logical 1 for INDIVIDUAL mode Ground or logical 0 for ERROR-SECONDS mode	Switch, 2 TTL inputs, 1KΩ to +5V
18	$\overline{10^6}$	Ground or logical 0 for 10^6 test length	Switch, 1 TTL input, 1KΩ to +5V
19	$\overline{10^7}$	Ground or logical 0 for 10^7 test length	Switch, 1 TTL input, 1KΩ to +5V
20	$\overline{10^8}$	Ground or logical 0 for 10^8 test length	Switch, 1 TTL input, 1KΩ to +5V
		All three at logical 0 or open for CONT test	
21	$\overline{\text{INSERT ERRORS}}$	Ground or logical 0 to insert errors	Switch, 1 TTL input, 1KΩ to +5V, .01μF to gnd
22	INTERRUPT DATA	Ground to open loop between Transmitter and Receiver	Switch, switch on input jack, 24KΩ to -5V, diode from gnd (not TTL compatible)
24,50	GND	Chassis ground and signal return	
25	+5V	+5V output for reference only (≤50mA)	
40	TRANSMITTER BIT SYNC	1.544 MHz Transmitter Clock, square wave	Transistor sw to gnd, 75Ω to +5V
41	TRANSMITTER WORD SYNC	Normally high, pulls to ground for 324 nsec once very 1,048,575 bits	Transistor sw to gnd, 75Ω to +5V
42	RECEIVER BIT SYNC	1.544 MHz Receiver Clock, square wave	Transistor sw to gnd, 75Ω to +5V
43	RECEIVER WORD SYNC	Normally high, pulls to ground for 324 nsec every 1,048,575 bits	Transistor sw to gnd, 75Ω to +5V
44	ERRORS	Normally high, pulls to ground for 324 nsec for each error received	Transistor sw to gnd, 75Ω to +5V
45	ERROR-SECONDS	Normally high, pulls to ground for 500 msec for each one-second block containing errors	Transistor sw to gnd, 75Ω to +5V
47	Carry	Normally low, goes to logical 1 for 10 msec when 3-digit error counter overflows	TTL output
48	Print	Normally low, goes to logical 1 for 100 msec at end of count interval	TTL output
50,24	GND	Chassis ground and signal return	

Reset/Resync, pin 15, must be driven by a buffer gate, contact closure, or transistor switch rather than by a standard TTL driver. This results from the requirement on the driver to sink 25 mA, which is equivalent to a fan-out of fifteen standard TTL loads.

Table 2-2: Remote Control Switch Positions

Switch	Position
MODE	
VIOLATIONS/ERRORS	ERRORS
INDIVIDUAL/ERROR-SECONDS	INDIVIDUAL
TEST LENGTH	
$10^6/10^7/10^8$/CONT/Timer	CONT
SELF TEST	
INTERRUPT DATA/NORMAL/ INSERT ERRORS	NORMAL

When the Test Set is under remote control, a new test may be begun, or a test in process may be aborted, by operating the Reset/Resync line. This is equivalent to operating the corresponding front panel switch. When resetting the Test Set, a ground should be applied to pin 15 for a period of not less than 10 msec. A new test will automatically start within 0.7 sec of the time when pin 15 is again open-circuited. The start of the new test will be signified by the lighting of the COUNT indicator and a logical 0 on pin 8 of the interface connector. If a ground is applied at pins 18, 19, or 20 the test will continue for 10^6, 10^7, or 10^8 bits respectively. A continuous or arbitrary test length may be achieved by leaving these three pins open-circuited. The test may be ended at any time by grounding pin 18, in which case the test will terminate within 0.7 sec of the application of this ground. The end of the test or count period will be signified by the extinguishing of the COUNT indicator on the front panel, the return on pin 8 to a logical 1, and the leading edge of the 100 msec print pulse on pin 48. The actual count period will always contain an integral number of words or 1,048,575 x N bits. The integer N can only be determined by monitoring the Receiver Word Sync signal on pin 43 of the Interface Connector.

2.4.2 Classes of Interface Signals and Circuits

2.4.2.1 Bindary-Coded Decimal (BCD) (Pins 1 through 6 and pins 26 through 31)

The three decimal digits of the internal error counter and display are brought out on these twelve interface lines. The information is presented in 1248, or BCD, code and all twelve outputs are in the inverted sense. These signals are buffered by TTL inverters located in the Auxiliary Module of the Test Set for the purpose of protecting the internal circuitry (ref. Figure 2-1); therefore, these lines are capable of sinking 16 mA and sourcing 400 μA, which is equivalent to ten standard TTL loads. Care should be taken to avoid conditions which exceed these current levels or cause the voltage applied externally to go beyond the range of 0 to +5 V dc.

2.4.2.2 Indicator Lights (Pins 7 through 13)

The information presented on the seven status indicators of the Test Set is duplicated in these seven signals. The information is presented such that a low level or logical zero is presented when the corresponding indicator is lighted. Like the BCD lines above, these are buffered by TTL inverters in the Auxiliary Module of the Test Set (ref. Figure 2-1). The electrical constraints listed in 2.4.2.1 apply.

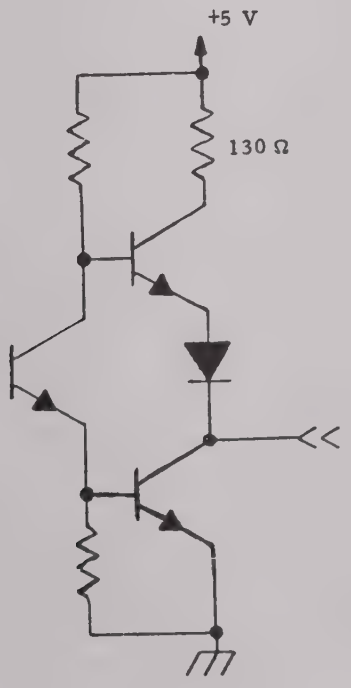


Figure 2-1: TTL Outputs

2.4.2.3 Control
(Pins 15 through 21)

These interface lines provide parallel access to the major front panel switches of the Test Set. They may, therefore, serve as outputs for monitoring switch settings or as inputs for remote control of the Test Set. If the front panel switches are set as listed in Table 2-2, +5 V will appear on all input lines and remote control may be affected via contact closures or NPN open-collector switching to ground.

These input lines are connected directly to one or more TTL inputs without input buffering (ref. Figure 2-2). The front panel switch to ground and a 1 KΩ resistor to the +5 V supply are also connected to these inputs. Any device driving these inputs must be capable of sinking current equal to 5 mA plus 1.6 mA times the number of TTL inputs indicated in Table 2-1. Since the 1 KΩ resistive pull-up is provided internally and the control lines may be shorted to ground by the front panel switch, the driving device should not be capable of sourcing current. The voltage of the inputs, including transients, must be restricted to betweeen ground and the internal supply, as provided on pin 25 of the Interface Connector.

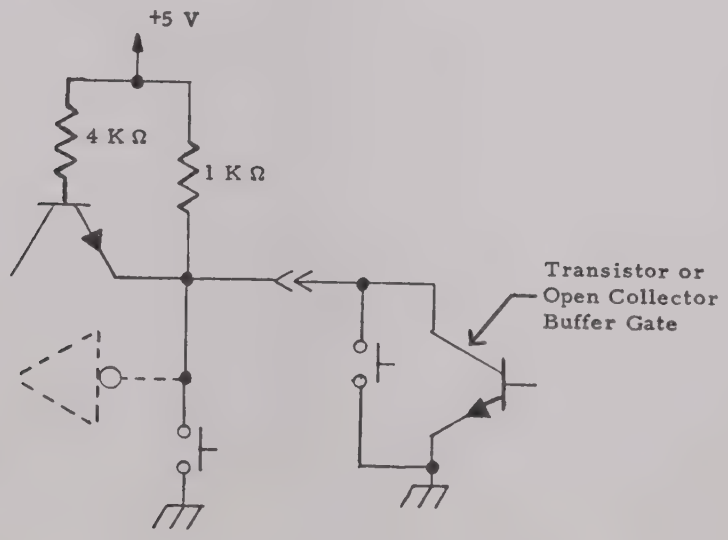


Figure 2-2: TTL Inputs

2.4.2.4 Interrupt Data Control
(Pin 22)

This control input is the only interface line which is not TTL compatible (ref. Figure 2-3). Tied to the input lines are two switches to ground, a 24 KΩ resistor to the -5 V supply, and a diode whose cathode is connected to ground. The two switches are the normally open controls of the SELF TEST switch and a set of normally open contacts on the DS1 INPUT jack. When all switches are open, this interface line is at approximately -0.7 V dc. The internal loop between the Transmitter and Receiver portion of the Test Set may be broken by grounding this control line through either a contact closure or an open collector PNP switching transistor.

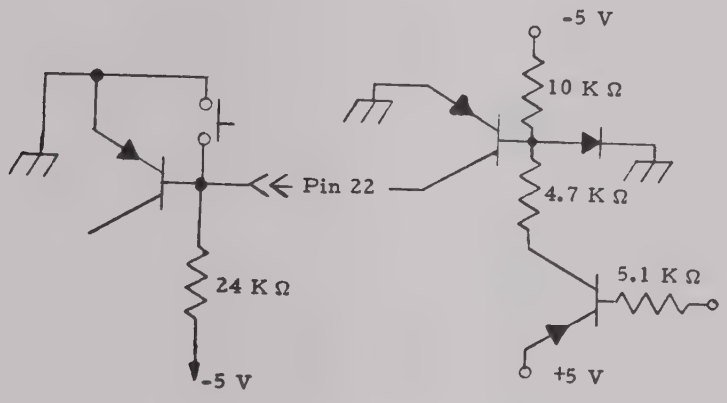


Figure 2-3: Interrupt Data Input

2.4.2.5 +5 V DC
(Pin 25)

The internal logic supply of the Test Set is provided on this pin of the Interface Connector for reference purposes. It should be used by the external interface circuitry to signify the maximum external voltage that can be tolerated at most of the TTL inputs and outputs. This includes the possibility in which the external circuitry is powered and the Test Set is not powered, or vice versa. The internal supply of the Test Set is not designed to power external circuitry requiring greater than 50 mA.

2.4.2.6 Auxiliary Outputs
(Pins 40 through 45)

The nature of these six signals is given in Section 1.3, Specification Summary, and their waveshapes are shown in Section 5.4, Figures 5-11 through 5-14.

The auxiliary outputs are derived from NPN transistor switches with 75 Ω pull-up resistors to the +5 V supply (ref. Figure 2-4). The transistors should not be required to sink more than 30 mA of current through the Interface Connector and the voltage must be restricted to between ground and +5 V. These outputs may be shorted to each other or to ground without danger of damage to the internal circuitry.

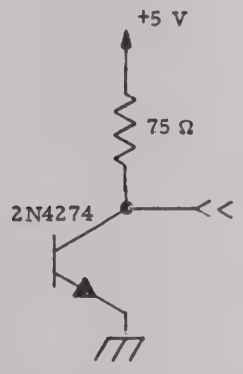


Figure 2-4: Auxiliary Outputs

2.4.2.7 Print and Carry Outputs
(Pins 47 and 48)

The carry output generates a 10 msec pulse each time the 3-digit display of the Test Set overflows. The 100 msec print pulse is generated at the end of each count interval when the COUNT indicator is extinguished. Both outputs are derived from TTL devices and normally remain low. Figure 2-1 and the restriction of par. 2.4.2.1 apply.

3.0 OPERATION AND APPLICATIONS

3.1 Controls, Indicators, and Jacks

Figure 3-1 shows the front panel with numbered callouts of all front panel controls, indicators, connectors, etc. Table 3-1 references the callouts numerically and includes the name and function of each.

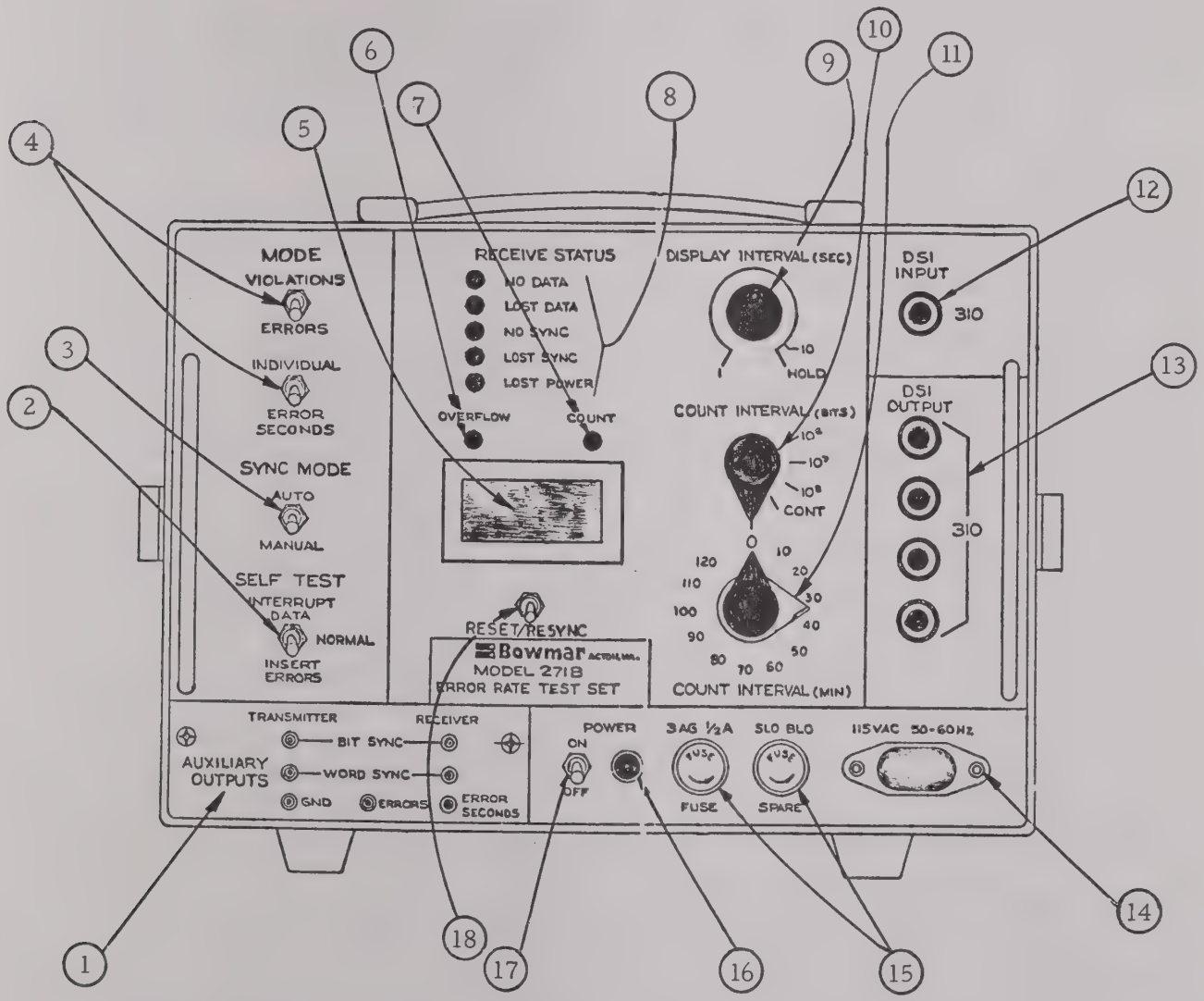


Figure 3-1: Front Panel Components
Error Rate Test Set

Table 3-1: Controls, Indicators, and Connectors

No.	Component	Description/Function
1	AUXILIARY OUTPUTS	Pin jacks that monitor the following six signals; one additional jack (GND) is provided for a ground connection. (a) TRANSMITTER BIT SYNC: a 1,544 MHz clock signal; square wave. (b) TRANSMITTER WORD SYNC: a pulse, 340 nsec long, generated once per full cycle of the transmitter sequence generator; changes this output's level from high to ground only for its duration. (c) RECEIVER BIT SYNC: the clock signal as taken from incoming data by the clock extractor circuit of the receiver. (d) RECEIVER WORD SYNC: a pulse, 340 nsec long, generated once per full cycle of the receiver sequence generator; changes this output's level from high to ground only for its duration. (e) ERRORS: a pulse, 340 nsec long, for every error detected by the receiver; changes this output's level from high to ground only for its duration. (f) ERROR-SECONDS: a pulse, 500 ±25 msec long, for every error-second; changes this output's level from high to ground only for its duration. An error-second is the occurrence of one or more errors within a one-second block of data.
2	SELF TEST Switch	A 3-position momentary switch used as follows. (a) NORMAL (center position): for normal operation of the Test Set. With no connection to the DS1 (receiver) input, the receiver and transmitter are

Table 3-1: Controls, Indicators, and Connectors

No.	Component	Description/Function
		directly linked. At the same time, if the MODE switch is set for ERRORS, all indicators will be off and the display will show no count. If the MODE switch is set for VIOLATIONS, the NO SYNC and LOST SYNC indicators will be held on while the NO DATA will be off, and the display will show no count. (b) INTERRUPT DATA (momentary up position): opens the link between receiver and transmitter, causing both the NO DATA and NO SYNC indicators to come on. Return to NORMAL will force the NO DATA indicator off. If the SYNC MODE switch is at AUTO, the LOST SYNC indicator will replace the NO SYNC upon return to NORMAL. This function is disabled when a plug is inserted into the DS1 INPUT jack. (c) INSERT ERRORS (momentary down position): inserts either logical errors or bipolar violations (depending on the MODE setting) into the transmitter test sequence. These errors appear at the DS1 (transmitter) output jacks and are directed to the receiver input via internal loopback wiring. In the receiver, these errors exercise detection and counter circuitry to be registered on the display. Since a known quantity of errors is injected into the receiver, this process provides a quick self-test.
3	SYNC MODE Switch	A 2-position toggle switch used as follows. (a) AUTO (up position): sets the Test Set for automatic resynchronization in the event that synchronization is lost. (b) MANUAL (down position): synchronization may be regained by operating the RESET/RESYNC switch.

Table 3-1: Controls, Indicators, and Connectors

No.	Component	Description/Function
4	MODE Switches	A pair of 2-position toggle switches used as follows. (a) VIOLATIONS/ERRORS: sets the Test Set for bipolar violations or logical errors; the transmitter is set for the type of errors it must insert in the quasi-random test sequence, and the receiver is set for the type of errors it must detect and count. (b) INDIVIDUAL/ERROR SECONDS: works independently of the VIOLATIONS/ERRORS switch by setting the receiver to count either individual errors or error-seconds.
5	Display	A 3-digit solid state indicator which presents a numerical readout of error count accumulated during any count interval.
6	OVERFLOW Indicator	A solid state indicator which is energized when the error count exceeds the numerical capacity of the display.
7	COUNT Indicator	A solid state indicator which is energized during error count intervals.
8	RECEIVE STATUS Indicators	Five solid state indicators for the following purposes. (a) NO DATA: is energized when data is not being presented to the receiver. (b) LOST DATA: is energized after data has been lost and subsequently regained; remains on until the RESET/RESYNC switch is activated. This indicator, with the NO DATA indicator, thus provides coverage of data loss from the instant of stoppage to the instant of manual resynchronization.

Table 3-1: Controls, Indicators, and Connectors

No.	Component	Description/Function
		(c) NO SYNC: is energized when the receiver is not synchronized to incoming data, or when the test set is in the VIOLATIONS mode. (d) LOST SYNC: is energized when receiver synchronization with incoming data has been lost and subsequently recovered; goes on when synchronization is recovered and remains on until the RESET/RESYNC switch is actuated. If the Test Set is in the VIOLATIONS mode, LOST SYNC will be held on. (e) LOST POWER: is energized as the Test Set is turned on, or when a power disturbance of sufficient magnitude to invalidate data is detected. In either case, it remains on until the RESET/RESYNC switch is actuated.
9	DISPLAY INTERVAL (SEC) Control	A variable potentiometer which determines the period of time the display will hold any given count; covers a range of from 1 to 10 seconds or continuous (HOLD).
10	COUNT INTERVAL (BITS) Switch	A 5-position switch whose settings determine the period of time, in bits, that counter circuits will count errors: 10^6; 10^7; 10^8; CONT, for continuous tally; or down, for use of the COUNT INTERVAL (MIN) timer. The first three positions should not be used for error-second measurements.
11	COUNT INTERVAL (MIN) Timer	A 0 to 2-hour mechanical timer, calibrated in minutes, which extends the range of fixable count intervals; its control knob is fitted with a secondary pointer to indicate initial setting.

Table 3-1: Controls, Indicators, and Connectors

No.	Component	Description/Function
12	DS1 INPUT Jack	A jack which accepts a WE 310-type plug; passes data from the system under test to the Test Set's receiver.
13	DS1 OUTPUT Jacks	Four jacks which accept WE 310-type plugs; serve as mutually independent outputs; each passes the transmitter output to a system under test.
14	115 VAC 50-60 HZ Power Input	A recessed male connector; mates with one end of the Test Set's power cord.
15	3AG 1/2A SLO BLO Fuseholders	Two fuseholders used as follows: (a) FUSE: holds the active power fuse. (b) SPARE: holds a spare fuse.
16	Power-On Indicator	A neon lamp which is energized whenever power is applied to the Test Set.
17	POWER ON/OFF Switch	A toggle switch which controls the application of power to the Test Set.
18	RESET/RESYNC Switch	A free-return toggle switch that resets the counter, initiates a new count, and resets LOST DATA, LOST SYNC, and LOST POWER indicators. In the ERRORS mode, this switch also initiates resynchronization and sets up a check of sync recognition circuits.

3.2 Applications

The Error Rate Test Set can be used to test any digital transmission system or system component accepting a DS1, T1-type, bipolar signal and returning a similar signal. While the Receiver of the Test Set is equivalent in application to Bipolar Violations (BPV) Detectors for testing T1 lines, its additional bit-by-bit error detection capability, using a long pseudorandom sequence, is intended to test those system components which remove bipolar violations and/or are capable of causing logical errors without causing

violations. The Transmitter of the Test Set is equivalent to and interchangeable with the Western Electric J98710R T1 Quasi-Random Signal Source and may be used independently of the Receiver for end-to-end tests or as a portable source. While the Transmitter provides a 3-volt bipolar signal for input at the cross-connect bay, the Receiver may operate at or up to 750 feet from the cross-connect bay or similar source, at the monitor jack, or at numerous points using a bridge adapter. The following gives specific applications of the Error Rate Test Set in testing T1 lines or circuits, T1 to T2 (M12) multiplexers, and modems.

3.2.1 The Error Rate Test Set may be used to test any T1 line using either its bipolar violations (BPV) or logical errors detection schemes. The only constraint on the choice of detection is that logical errors detection requires the use of the standard test sequence whereas bipolar violations detection may be applied to any signal. An example of the latter type of detection, using message/data as the signal, would be the in-service monitoring of a circuit without the necessity of removing it from service. Figures 3-1 (a) and (b) depict typical applications of the Error Rate Test Set for checking T1 lines in both loopback and end-to-end configurations.

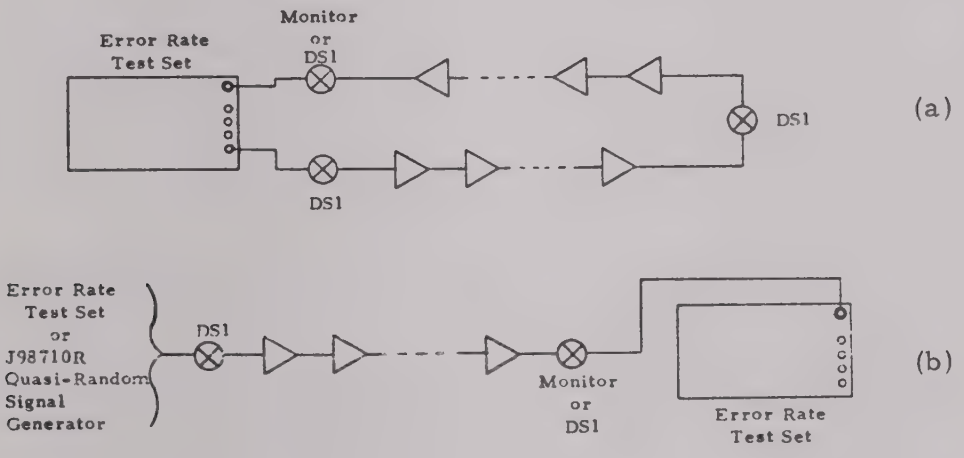


Figure 3-1: Loopback and End-to-End Applications

Traditionally, the Bell System J98710F Fault Locating Set (10F) has been used as a signal source when checking T1 lines, particularly during the acceptance testing that follows final construction, rerouting, or major repairs. If a line contains a splicing error, known as a double split, or if it contains other equally serious problems, the line will pass all checks using a 10F but it will not support a terminal. The Error Rate Test Set will show such a line to be faulty because its quasi-random pattern stresses

the line more realistically. It is therefore recommended that checkout with an Error Rate Test Set be added to Local Practices for line testing.

3.2.2 In some instances, idle circuits in an office may carry the standard test pattern merely to provide signal excitation. The Error Rate Test Set, used as a signal source, may be instructed to insert a fixed rate of either logical errors or bipolar violations into the test pattern sequence at a rate of approximately 8×10^{-6} in order to verify circuit identification. Added to the actual errors, such an increase can be recognized on most circuits.

3.2.3 Multiplexers and modems interfacing DS1, T1-type, signals to either higher order digital systems or analog systems are capable of removing bipolar violations from their inputs and/or can cause logical errors without violations appearing in the output data. It follows that the same is true of systems such as intercity spans, if they contain these components anywhere between their end points. The pseudo-random sequence and logical errors detection make it possible to evaluate such systems. It should be noted that BPV testing is not adequate for such systems as only the near-end bipolar equipment will be tested by BPV techniques. As an example, consider the DS1 to DS2, T1 to T2 (M12) multiplexer which combines four DS1 data streams into one DS2 stream. While the test sequence is needed only for the channel under check, the Error Rate Test Set provides four identical outputs to identically stress all four channels of the multiplexer. Not only are loopback and end-to-end tests possible, but tests over the higher order system or analog medium are also possible, as depicted in Figures 3-2 (a) and (b).

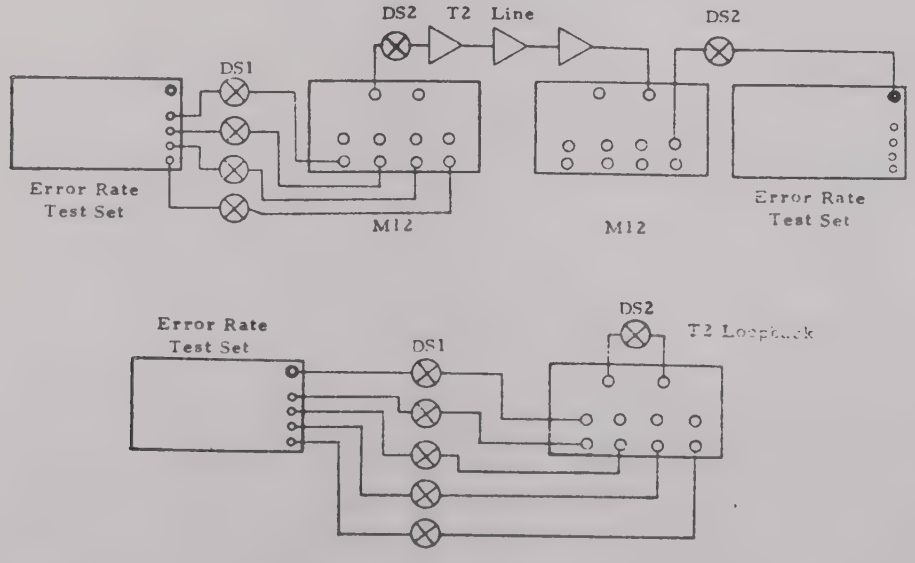


Figure 3-2: Higher Order System and Analog Medium Applications

4.0 THEORY OF OPERATION

4.1 General

Refer to the block diagrams, Figures 4-1 and 4-2, and the schematics of Section 6 to correlate descriptions of this section.

4.2 Transmitter

The Transmitter portion of the Error Rate Test Set is a DS1 (T1) type test source. Its output is a continuously repeating sequence of data bits in a quasi-random arrangement, identical to the output of the Western Electric J98710R T1 Quasi-Random Signal Source. The output supplied by each of four independent jacks is a 1.544 Mbps, 3 V peak, bipolar, return-to-zero (RZ) signal with trailing edge overshoot. Its quasi-random sequence of 1,048,575 data bits is derived from a self-starting Sequence Generator.

The Error Rate Test Set's 1,048,575 bit test pattern differs from the Sequence Generator's 1,048,575 bit natural pattern in the length of the consecutive-zero runs. The natural pattern contains several strings of long 0 runs; however, monitoring circuitry attached to the Sequence Generator is set to react to a count of fifteen consecutive 0's. When this count is detected, the Invert Data Gate at the output of the Sequence Generator is activated to convert the first 0 of the run to a 1 as it is shifted into output circuitry. This process continues with each shift until the run in Generator stages is less than fifteen 0's long. Thus, a fourteen-zero limit is imposed on all strings of consecutive 0's in the Test Set's test pattern.

For purposes of self-test and the test of other systems, the Test Set can be made to insert a fixed number of errors into each cycle of the Transmitter test pattern. A mode switch offers a choice of either logical errors or bipolar violations. Their insertion into the test pattern is then dependent upon the detection of seventeen or more consecutive 0's, which occurs four times per 1,048,575 bit cycle. A pair of errors is inserted at each of the four insertion times, so that four pairs are inserted into each cycle of the test pattern.

Each of the four instances of logical-errors insertion per cycle of test pattern is simply the conversion of two data bits to their alternate configurations - a 0 is converted to a 1, and a 1 is converted to a 0. Conversion is effected by temporarily altering the function of the circuitry that imposes the fourteen-zero limit on the Sequence Generator's output. Though this circuitry is momentarily altered, the fourteen-zero constraint is maintained and bipolar format is unchanged.

Bipolar violations are inserted by temporarily inhibiting the circuitry which converts the test pattern to bipolar format (alternating the polarity of each

consecutive 1). The process is applied on a series of four 1's in a manner that produces two consecutive bits of one polarity followed by two consecutive bits of the opposite polarity; thus, a pair of bipolar violations is produced. The series of four 1's is made available by circuitry which imposes the fourteen-zero constraint on the output of the Sequence Generator.

Table 3-1 illustrates a condition of seventeen or more 0's within the Sequence Generator and the effects of fourteen-zero constraint and errors insertion. A Sequence Generator content of eighteen 0's is depicted, followed by the effects of fourteen-zero constraint and normal conversion to bipolar format. The bipolar sequence is then shown as it would appear after insertion of logical errors and after bipolar violations. The time scale is from left to right, so that initial bits of the sequence are at the left.

Table IV: Test Set Treatment of Seventeen Consecutive Zeros

Description	Data Stream Segment
Any condition of 17 or more zeros (18 shown) in Sequence Generator output:	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
Corrected output (without errors):	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
Corresponding Transmitter output, bipolar format:	+ - + - + 0 0 0 0 0 0 0 0 0 0 0 0 0 0 -
Corresponding Transmitter output with logical errors:	0 + - + - + 0 0 0 0 0 0 0 0 0 0 0 0 0 0 -
Logical errors:	X X
Corresponding Transmitter output with bipolar violations:	+ + - - + 0 0 0 0 0 0 0 0 0 0 0 0 0 0 -
Bipolar violations:	X X

4.3 Receiver

Evaluation of data from a system under test takes place in the Receiver. Incoming data, in bipolar format, is first sliced at its half-peak amplitude level, then sampled at the center of each bit period. A Peak Detector provides automatic threshold control for the Slicers.

Clock pulses for the Receiver are taken directly from the reshaped data by a Clock Extractor circuit. When data is discontinued or interrupted, a No Data Detector signals the NO DATA indicator and inhibits Clock pulses to data processing circuits.

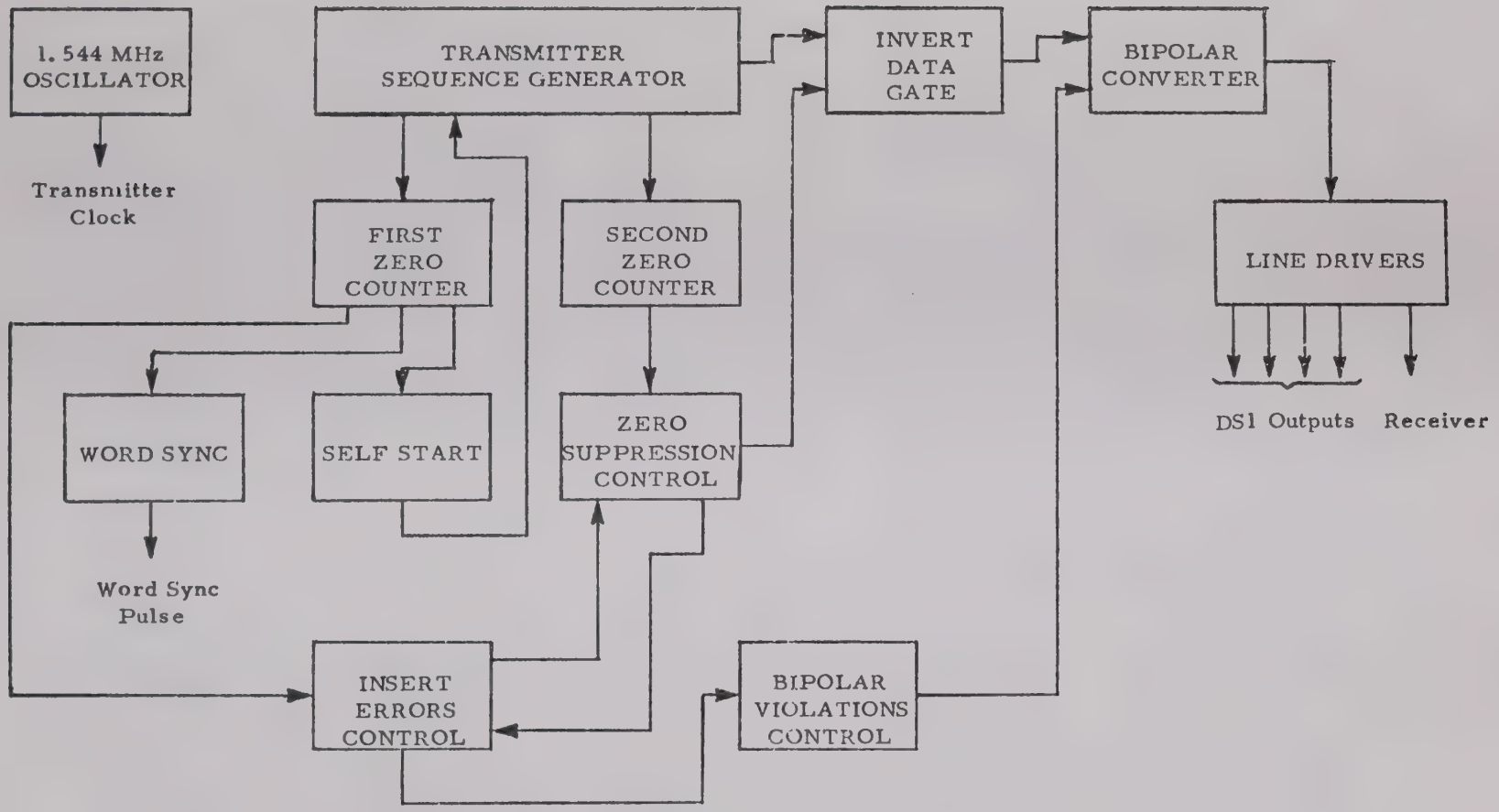


Figure 4-1: Transmitter Section Block Diagram
Transmitter Module (A5)

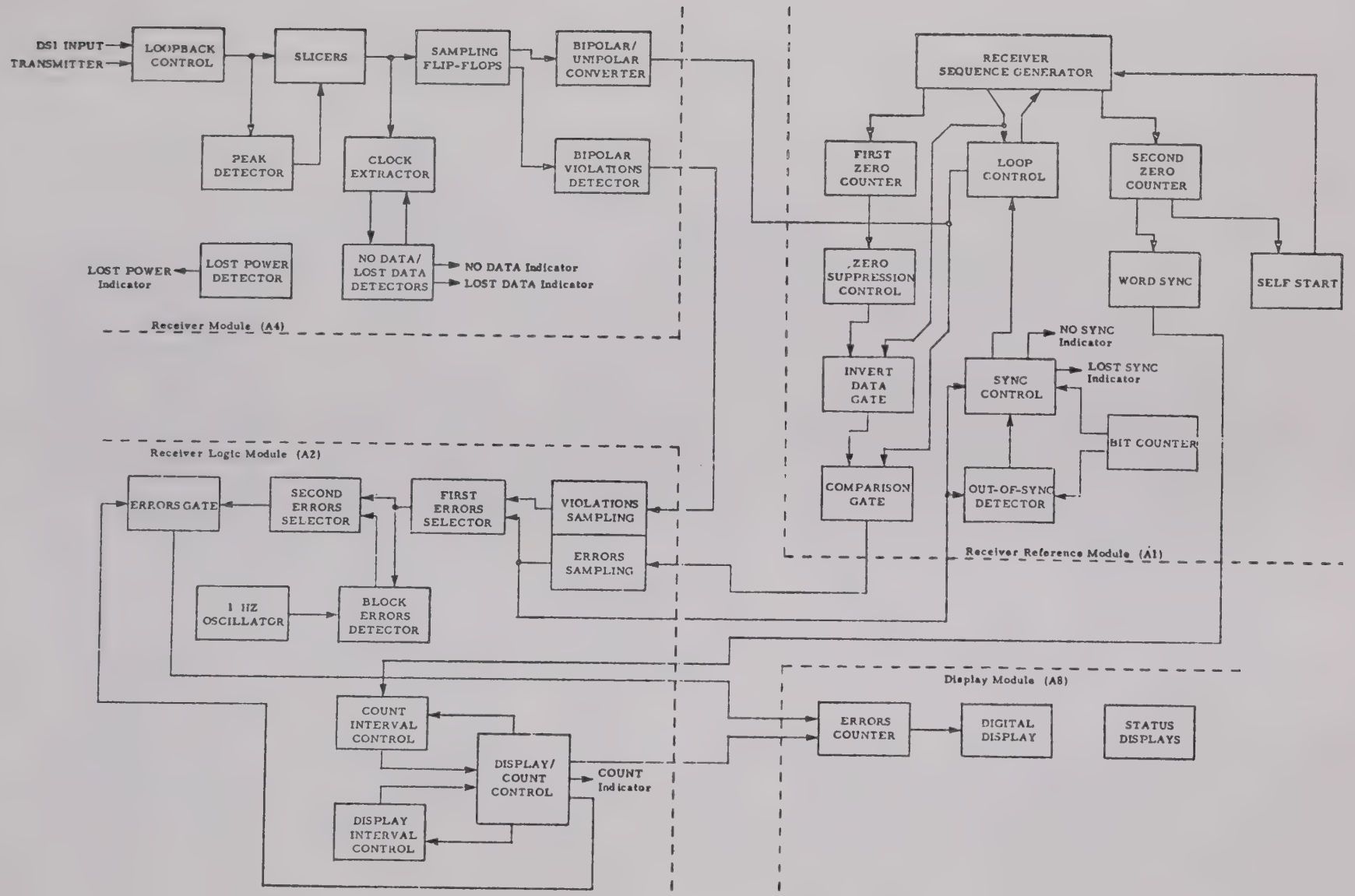


Figure 4-2: Receiver Section Block Diagram

Reshaped and sampled data is directed to the Bipolar Violations Detector and the Bipolar/Unipolar Converter. The first circuit looks for two consecutive 1's of the same polarity, while the second circuit converts data from bipolar to unipolar format. The outputs of these two circuits are then ANDed. If the VIOLATIONS/ERRORS mode switch is set for ERRORS, the received data, in unipolar format, is routed to the Receiver Sequence Generator. This Generator differs from its Transmitter counterpart only in its monitor points and in a modified feedback loop; otherwise, it is capable of the same 1,048,575 bit test pattern. Its purpose is to provide a base pattern for checking the incoming unipolar data for logical errors by a process described in later paragraphs.

If the VIOLATIONS/ERRORS mode switch is set for VIOLATIONS, unipolar data is ignored, and the output of the Bipolar Violations Detector is forwarded directly to the Error Counter or the Block Error Detector. In this situation, the Receiver Sequence Generator is made to continuously cycle simply to provide a time base for test length selection via the COUNT INTERVAL (BITS) switch. When operating in this capacity, the Sequence Generator is self-starting, but it does not attempt to synchronize to the unipolar data stream.

The key difference between the Transmitter and Receiver Sequence Generators is the latter's modified feedback loop, which is arranged to be open or closed. When it is closed the two generators behave identically, as self-starting generators for the 1,048,575 bit test pattern; when it is open it is injected with the unipolar data stream. If the unipolar data contains no errors, it deceives the Receiver Sequence Generator into behaving as a closed loop device, thus synchronizing it with the incoming data.

Synchronization of incoming unipolar data with the Receiver Sequence Generator may be initiated automatically or manually, depending on the setting of the SYNC MODE switch. In the MANUAL mode, loss of sync is made apparent by the NO SYNC indicator; resynchronization is gained by actuating the RESET/RESYNC switch. Once synchronization is achieved and the Sequence Generator loop is closed, the Generator output becomes its own natural pattern. The incoming unipolar data is then compared with this output and checked for logical error content. Detected errors are monitored by the Errors Counter or Block Errors Detector for subsequent accounting via the Display.

If the INDIVIDUAL/ERROR-SECONDS mode switch is set at ERROR-SECONDS, logical errors or bipolar violations, as selected, pass through a Block Error Detector before being directed to the Errors Counter. The Block Error Detector is limited to a maximum count rate of one per second, therefore, the COUNT INTERVAL (BITS) switch should be set at either its CONT or Timer position for a meaningful count.

If the INDIVIDUAL/ERROR-SECONDS mode switch is set at INDIVIDUAL, error pulses bypass the Block Errors Detector and appear directly at the Errors Counter. In this mode, the Display shows errors per one, ten, or one hundred cycles of the test sequence by selection of the 10^6, 10^7, or 10^8 positions respectively of the COUNT INTERVAL (BITS) switch. CONT or Timer positions are used for MANUAL mode operation or for very long intervals.

4.4 Transmitter Circuits (A5 Module) (Pages 6-15, 6-16)

4.4.1 1.544 MHz Clock

A 3.088 MHz crystal oscillator (Q1, Q2) is divided by a single JK flip-flop (IC17A) to provide a 1.544 MHz symmetrical 2-phase clock. Q3 and Q4 serve as an emitter-follower and a buffer; Q1 and Q2 act as a 2-transistor amplifier with negative feedback, with Q1 providing most of the gain. Negative feedback stabilizes the bias points and holds crystal current to a good operating range. Positive feedback through the crystal is sufficient to produce oscillation, which occurs at the frequency of minimum crystal impedance (the series-resonant frequency). Resultant Clock pulses are distributed throughout the Transmitter to control all timing functions.

4.4.2 Transmitter Sequence Generator

Quasi-random test patterns, or sequences, issued by the Transmitter are derived from a 20-stage shift register generator whose feedback is taken from stages 17 and 20. The Generator is contained by IC1A through 4B, with feedback directed through the exlusive-OR circuit of IC8B.

The Sequence Generator provides a continuously repeating sequence of 1's and 0's. Each sequence is made up of all but one of the 2^{20} possible combinations of 20-bit states, for a total of 1,048,575 bits. The one exception is the all-zero state in which the Generator, by nature of its circuitry, will not function. The all-zero state is eliminated by Zero Suppression Control circuitry during normal operation. In a situation where all-zeros might occur, a Self Start circuit (ref. 4.4.4) is available to respond with injection of a 1 to unlock the Generator. During normal operation, the maximum count of 0's in the generator is nineteen.

The main output of the Generator is taken from the 20th stage. Auxiliary outputs from the 2nd, 5th, 6th, and 7th stages enable monitoring of the serial progression of bits through Generator stages for purposes of determining need for self start, zero suppression, error insertion, etc. Each generated bit shifts a stage at a time with each Clock pulse.

Since auxiliary outputs are several stages ahead of the main output, they offer a preview of the output sequence of bits. This feature permits the necessary advance notice required for such actions as the fourteen-zero constraint, or

the seventeen or more 0's state for error insertions, etc. Specific purposes of these outputs are described in paragraphs that follow (ref. par. 4.4.7, 4.5.2.3, 4.5.2.5).

4.4.3 Transmitter Zero Counters

Two separate counters are connected to auxiliary outputs of the Sequence Generator to register any series of successive 0's. Both counters are actually incremented by Clock pulses, but each is reset by registration of a 1 so that accumulated counts represent a series of 0's.

The First Zero Counter (IC13A, 5A, and 7A) is a 5-bit binary type, connected to the 2nd stage auxiliary output. It is used to aid the Self Start circuit (ref. 4.4.4) in providing a sync pulse at the beginning of each cycle of test sequence, and in controlling error insertion.

The Second Zero Counter (IC6) has four stages and is tied to the 5th stage auxiliary output, which is three stages behind the 2nd stage tap. This Counter signals the Zero Suppression Control (ref. 4.4.7) when it has registered fifteen consecutive 0's.

4.4.4 Transmitter Self Start

Self starting is initiated through a single gate (IC10A) by a count of twenty-four from the First Zero Counter (ref. 4.4.3). This count is possible only if the Sequence Generator is locked into the all-zero state and Clock pulses continue to increment the First Zero Counter. The only opportunity for all-zero lock-up and self starting occurs when the Error Rate Test Set is switched on for use. After power is turned on, the possibility for all-zero lock-up is eliminated by Zero Suppression Control circuitry, which limits strings of successive zeros to less than the critical level of twenty.

As described earlier, the Sequence Generator cannot function in an all-zero state, therefore, upon registration of twenty-four 0's by the First Zero Counter, the Self Start circuit is activated to force a single 1 into the input of the 2nd stage of the Generator. This resets the Counter and stimulates the Generator into normal operation.

4.4.5 Transmitter Word Sync

A single gate (IC9B) with an inverter (IC13D) makes up the Transmitter Word Sync circuit. This circuit is connected to the First Zero Counter to respond to passage of nineteen 0's and a 1 through the Sequence Generator's 2nd stage. Since this condition occurs only once every 1,048,575 bits, (a full cycle of the test pattern) it is used to mark each test pattern cycle. The response is a sync pulse to the TRANSMITTER WORD SYNC test point.

4.4.6 Insert Errors Control

Error injection into the test pattern is accomplished by holding the SELF TEST switch at its INSERT ERRORS position. A choice of logical errors

or bipolar violations is made by setting the VIOLATIONS/ERRORS mode switch to ERRORS or VIOLATIONS respectively. Errors are injected at a point beyond the Sequence Generator output. Insertion is triggered by the First Zero Counter's detection of seventeen or more consecutive 0's. This condition occurs four times during each cycle of the test pattern. In each instance, a pair of errors, rather than a single error, is inserted so that both a 1-to-0 and a 0-to-1 conversion is accounted for; thus, four pairs of errors are injected for each cycle of the test sequence.

The Insert Errors Control circuitry is made up of several gates and inverters (IC9A, 13C and E, 14D, 18A through C, 19A through C) and a flip-flop (IC15A). The count of seventeen 0's is detected by IC9A and is used to set the flip-flop. Remaining gates then act as steering circuits, enabling the Insert Errors Control to activate either the Zero Suppression Control or the Bipolar Violations Control (ref. 4.4.7, 4.4.8) for insertion of the desired type of error.

4.4.7 Transmitter Zero Suppression Control

This circuit is situated along the path of the Sequence Generator output. Unless activated, it simply passes data bits of the Generator's test pattern without alteration. When activated, it can convert each data bit it passes from a 0 to a 1, or a 1 to a 0, depending on the purpose of its activation. It is made up of gates and inverters (IC10B, 11A through D, 14A through C) and a flip-flop (IC15B).

The Zero Suppression Control may be activated for one of two purposes. First, it is the final link in circuitry that imposes the fourteen-zero restraint in the test pattern and, second, it is used to force logical errors into the test pattern. Both purposes are discussed more fully in the two paragraphs that follow.

Activation of the Zero Suppression Control for fourteen-zero constraint occurs after the registration of fifteen 0's by the Second Zero Counter, which monitors the Sequence Generator's 5th stage output. A count of fifteen by the Second Zero Counter indicates a string of 0's extending from stages 5 through 19 of the Sequence Generator. At the very next Clock pulse, the fifteen 0's are all shifted one stage ahead to occupy stages 6 through 20, while the Zero Suppression Control circuit is activated to convert the 0 at the output of the 20th stage to a 1. Thus, the fifteen-zero string will continue to increment the Second Zero Counter and to activate the Zero Suppression Control, so that zero suppression continues until a 1 appears in the 5th stage to end the string and reset the counter.

Operation of the Zero Suppression Control is modified slightly when logical errors are to be inserted. As discussed in par. 4.4.6, errors are inserted in the test pattern when a string of seventeen or more 0's occurs in the Sequence Generator. This string is monitored at the Generator's 2nd stage by the First Zero Counter. At the count of seventeen, the string occupies stages 2 through 18, and at the very next Clock pulse the string is shifted to stages 3 through 19 while the Zero Suppression Control is activated. Actually, activation of the

Zero Suppression Control is triggered by signals from the Insert Errors Control and the First Zero Counter together. Action of the Zero Suppression Control, however, is on the bit in the Generator's 20th stage and not on the first 0 of the string located in the 19th stage. The bit in the 20th stage is a 1 and it is converted to a 0, thus creating an error in the test pattern. At the next three Clock pulses, the first three 0's of the seventeen-zero string are converted to 1's in the usual manner of zero suppression; then, through the action of steering gates in the Insert Errors Control, the Zero Suppression Control is held on for an additional Clock pulse in order to convert an extra 0 to a 1. This latter action introduces the second and final error for the seventeen-zero string. The net result of the two error insertions is a 1-to-0 conversion and a 0-to-1 conversion.

The following table is a representation of Sequence Generator contents and its conversion, with and without errors.

Table V: Conversion of Seventeen-Zero Generator String

Sequence Generator	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Normal output	1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Output with errors	0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	↑ 1st error ↖ 2nd error
	Time

4.4.8 Bipolar Violations Control

The rate at which bipolar violations are added to the pattern is controlled in exactly the same manner and by the same circuitry as the Insert Errors Control (ref. 4.4.6). Violations are created by inhibiting the toggle action of the Bipolar Converter flip-flop (IC7B). This inhibit signal is generated by the action of IC21A and 12B.

IC21A is connected as a 3-bit binary counter. The output of the first stage of this counter is connected to the input of a D-type flip-flop (IC12B). This flip-flop is clocked by the Phase 1 Transmitter Clock to provide proper timing. A reset signal is taken from the third stage of this counter, which indicates the completion of the fourth counting period. This signal resets both the Insert Errors Control and the Bipolar Violations Control circuits.

Initially, all circuits are maintained in a reset condition. Upon detection of seventeen consecutive 0's, the reset control is removed, permitting IC21A to count Transmitter Clock pulses. During the second clock pulse period, the input to IC12B is held at logical 1. IC12B is then clocked during the middle of this period, producing the inhibit signal which is directed to IC7B. This sequence of operation continues through the next two Clock periods. No inhibit is generated during the third period, but is is present during the fourth period. This results in two violations separated by one nonviolated data bit. At the end of the fourth period, the circuitry returns to its reset condition until the next sequence of seventeen consecutive 0's.

4.4.9 Invert Data Gate

This circuit is an exclusive-OR gate (IC8A) through which the Zero Suppression Control inverts output bits of the Sequence Generator. The output of IC8A is sampled and delayed one-half bit by the sampling flip-flop (IC12A). This delay eliminates transients which result from the simultaneous switching of the many circuits controlled by Clock pulses. The output of the flip-flop is then ANDed with Clock pulses through IC16A to obtain a RZ data format for the Bipolar Converter (ref. 4.4.10).

4.4.10 Bipolar Converter

A single flip-flop (IC7B) and four gates (IC16C and D, 8C and D) make up the Bipolar Converter. Its function is to alternate the polarity of all 1's in the test sequence, regardless of the interspersion of 0's; thus, when a 1 is generated of one polarity, the next 1 will have the opposite polarity, whether or not there are 0's between the two 1's.

Bipolarization is triggered by the trailing edge of each 1 in the data stream. At this instant, the flip-flop toggles so that the next 1 is transmitted with the opposite polarity. Two gates, IC8C and D, delay the toggle input to the flip-flop slightly to ensure a correct time relationship with the inhibit input from the Bipolar Violations Control Circuit.

The output of the Invert Data Gate is ANDed with each of the toggle flip-flop outputs to provide necessary steering for the Line Drivers (ref. 4.4.11). The toggle flip-flop must not operate during insertion of a bipolar violation and it is, therefore, momentarily disabled by the Bipolar Violations Control (ref. 4.4.8).

4.4.11 Line Drivers

Each of the Bipolar Converter's two outputs is directed to paralleled pairs of driver transistor switches (Q5, Q6 and Q7, Q8) whose outputs are tied to an outer tap of a center-tapped transformer primary (T1). The paralleled transistor switch arrangement ensures a higher speed of operation and higher current capacity. One switch pair with half the primary handles positive bits of the bipolar signal, while the other pair and half primary handle negative bits.

The transformer is trifilar wound, with two of its windings connected as the center-tapped primary. The third winding serves as the balanced output, which is padded as necessary and distributed to the DS1 OUTPUT jacks and to the Receiver. Shaping of the inherently rectangular signal bits into the T1 pulse shape with trailing edge overshoot is accomplished with a passive RLC circuit (R21, 22; L1; C10) connected across the transformer primary.

4.4.12 Pads

The output of the Line Drivers (ref. 4.4.11) is connected to a parallel arrangement of pads, which serves to drop the output voltage to 3 volts while providing a measure of isolation between outputs. Four pads link the line drivers to the DS1 OUTPUT jacks; a fifth pad of higher attenuation provides a loopback path from the Transmitter to the Receiver for self test purposes. The output of each of the five pads is arranged to terminate in 100 ohms when not in use by the jack switch. This presents a constant impedance to the Line Drivers' pulse-shaping network, regardless of outputs in use.

4.5 Receiver Circuits

4.5.1 Receiver Module (A4) (Pages 6-13, 6-14)

4.5.1.1 Loopback Control

Loopback between Transmitter and Receiver is controlled by a reed relay (K1) and its coil driver (Q1, 2). The loop is normally closed, and is opened by insertion of a plug into the DS1 INPUT jack or by holding the SELF TEST switch at its INTERRUPT DATA position. The relay is de-energized when the loop is open.

4.5.1.2 Peak Detector

To accommodate bipolar inputs of widely varying amplitudes, a Peak Detector circuit supplies a threshold level to the Slicers (ref. 4.5.1.3). This circuit is a full-wave type which effectively converts its bipolar inputs to unipolar. Its output is taken from a voltage divider which, coupled with C3, supplies a level half the peak amplitude of each incoming 1 bit. Q3, 4 and R10, 11 make up the Detector.

NOTE: Transistors Q3, 4, 5, 6 and diode CR2 are contained in a single monolithic device (IC16). This single device was chosen over separate transistors to take advantage of the closely matched temperature coefficients of transistors residing on a single substrate. (Applies to units with Receiver Assembly C271-225, Rev. D and higher.)

4.5.1.3 Slicers

A pair of Slicer circuits compares the outputs from the transformer secondaries to the output of the Peak Detector to establish a peak level for each incoming 1 bit. Bits of one polarity are handled by Q5 in conjunction with IC5A and B, while bits of the opposite polarity are handled by Q6 in conjunction with IC5D and C. A separate output for each polarity preserves the polarity information for the Bipolar Violations Detector. The entire function is performed by a dual line receiver, which provides high-speed operation with little offset error.

4.5.1.4 Clock Extractor

The Receiver derives clock pulses from incoming data, rather than from an internal clock, so that it can properly synchronize with incoming signals. The Clock Extractor monitors, and effectively rectifies, both Slicer outputs through IC6A and Q7. The rectified signal is then converted into a series of pulses, a pulse for each 1 bit, which is applied to a very high-Q circuit (L1 and C7). The result is a ringing output of more than adequate duration to supply Clock pulses during strings of 0 bits of the maximum allowable length; thus, a 1.544 MHz frequency component is extracted from the received signal regardless of 0 bits.

The output of the high-Q circuit is phased as required and applied to a separate slicer (IC7A) for shaping. The final output is a symmetrical clock signal of proper phase for the entire Receiver.

4.5.1.5 No Data/Lost Data Detectors

These two circuits provide coverage of data loss from the instant of stoppage to the instant of manual resynchronization. The No Data Detector provides visual warning via the NO DATA indicator when data is not being presented to the Receiver. The Lost Data Detector shows loss of data via the LOST DATA indicator, which goes on with the return of data and remains on until the RESET/RESYNC switch is activated.

The No Data Detector, consisting of IC9 monitors the output of the slicers through IC6A. The dual retriggerable monostable multivibrator IC9 is connected in a tandem arrangement, where the second stage is triggered by an output of the first. The first stage is continuously retriggered by data pulses from the output of IC6A. In the event that data is interrupted, retriggering is discontinued, permitting this stage to complete its monostable function. The time constant of the first stage (26.5 microseconds) is determined by circuit elements R57 and C26. This time constant corresponds to 41 ± 9 zeroes, which defines the No Data threshold. The second stage, when triggered by the No Data condition detected by the first stage, generates a pulse of 100 ± 20 ms. An output from this stage is applied to the gate input of the first stage which inhibits triggering of the first stage for a 100 ms period following detection of No Data. The 100 ms time constant is determined by components R56 and C28. The output of the No Data circuit is extracted from the first stage. This output is directed to both the No Data indicator buffer through IC6D and to the clock extractor circuit IC7B. Flip-flop IC8A controls the LOST DATA indicator. It is set whenever the NO DATA indicator goes off and is reset only by actuation of the RESET/RESYNC switch.

4.5.1.6 Sampling Flip-Flops

Positive and negative data bits from the outputs of the slicers (IC5B and D) are channeled to the input of two D-type flip-flops (IC1A and B respectively). Sampling is achieved by clocking these flip-flops with the receive data clock (ref. 4.5.1.4).

4.5.1.7 Bipolar/Unipolar Converter

Conversion to a unipolar NRZ (nonreturn-to-zero) format is accomplished by ORing together the outputs of sampling flip-flops IC1A and B. The OR function is provided by IC3A.

4.5.1.8 Bipolar Violations Detector

This circuit consists of two 2-stage binary counters (IC2A, 2B and IC4A, 4B). A gate for each counter ANDs the Receiver Clock pulses with a Slicer output to give RZ signals which toggle and reset the counters. When a 1 of positive polarity is received, the first stage of one counter is set and the second counter is cleared. If the next 1 received is also of positive polarity, another count will be added to the first counter, indicating the occurrence of a violation; however, if the next 1 had been of negative polarity, this counter would have cleared and a count of one would have registered in the first stage of the second counter.

ORing the two counter outputs and ANDing the result with the unipolar data stream completes the bipolar violations detection process. The resultant violations data is channeled to the Error Counter for subsequent display, provided the VIOLATIONS/ERRORS switch is set for VIOLATIONS.

4.5.1.9 Lost Power Detector

The Lost Power Detector monitors the +5 volt supply for excursions of 1/2 volt or more below the +5 volt level; 4.5 volts is the minimum level at which the Test Set can function normally. The occurrence of such excursions causes this circuit to turn on the LOST POWER indicator, which can be cleared only by actuating the RESET/RESYNC switch. This circuit

responds to either a long-term loss of power or a severe power disturbance, and warns the operator to check the data for possible errors.

Components of this circuit are CR4, Q16, Q15, and IC14A and B. IC14A and B form a set-reset flip-flop which will always shift to the set state when power is applied, at which time the LOST POWER indicator comes on. Setting potentiometer R61 for a 3.8 volt drop between its center tap and the terminal attached to the +5 volt supply rail enables Q16 to turn off when the output of the +5 volt supply falls below 4.5 volts. Upon turn-off of Q16, Q15 turns on and shorts C27, which sets the flip-flop; in turn, the flip-flop activates the LOST POWER indicator.

4.5.2 Receiver Reference Module (A1) (Pages 6-7, 6-8)

4.5.2.1 Receiver Sequence Generator

The Receiver Sequence Generator produces a test sequence identical to that of its Transmitter counterpart (ref. 4.4.2). Its outputs are taken from different stages of the shift register, its timing is derived by extracting clock pulses from incoming data, and its feedback loop may be opened to receive incoming data for the purpose of synchronization with this data. Generator components are IC1, 2, 17A and B, 18A and B; IC19A serves as the exclusive-OR circuit in the feedback link. The bridge between stages 17 and 18 contains the Loop Control circuitry (ref. 4.5.2.2) which opens or closes the feedback loop. The intent of different output locations is explained in paragraphs that follow, the clock pulse extraction was discussed in par. 4.5.1.4, and manipulation of the feedback loop is described below.

With the feedback loop closed, the Receiver Generator behaves exactly as the Transmitter Generator in working up the 1,048,575 bit test sequence, but it is necessary to synchronize the test sequence from the Receiver Generator with that of an incoming signal if a bit-by-bit comparison of data bits is to be performed. This synchronization is achieved by opening the feedback loop and inserting the incoming signal in place of the Generator's output. The Generator responds as if the loop were closed, and within a very brief time interval (twenty data bits later), the Generator's output corresponds exactly with the data being inserted in its place.

Should incoming data contain error bits during synchronization, the process will be delayed. In order for synchronization to be achieved, incoming data must contain at least twenty error-free bits; an additional forty error-free bits must be received in order to confirm synchronization. Once synchronization is confirmed, the Generator's Sync Control circuit (ref. 4.5.2.10) forces the feedback loop to its closed status so that normal operation may resume.

Should synchronization be lost during normal operation, the loss is detected

by the Out-of-Sync Detector (ref. 4.5.2.9). In the AUTO mode, this circuit then signals the Sync Control to reopen the feedback loop for resynchronization. Resynchronization in the MANUAL mode is initiated by actuating the RESET/RESYNC switch.

4.5.2.2 Loop Control

A gate system (IC13A, B, and C) effectively forms an SPDT switch which controls the Receiver Generator's feedback loop. The input to stage 18 from IC13B is the common line. When the loop is closed, stage 18 receives data directly from the output of stage 17; when the loop is open, it receives the incoming unipolar data signal. Should synchronization be required, the Sync Control (ref. 4.5.2.10) may force the Loop Control to switch stage 18 to the incoming data line through an inverter (IC11F). If the Generator is properly synchronized to incoming data, there will be no signal from the Sync Control, and the Loop Control will therefore switch data from stage 17 to stage 18.

4.5.2.3 Receiver Zero Counters

Two Zero Counters are connected to the Receiver Sequence Generator. Their function and operation are identical to the Transmitter Zero Counters (ref. 4.4.3). The First Zero Counter is a 4-bit binary counter (IC6) which monitors the output of stage 1 and limits the number of consecutive 0's in the Receiver Generator's test sequence. The Second Zero Counter is a 5-bit device (IC8, 12B, 19C) which is connected to the Generator's 19th stage output. It makes the Generator self-starting for bipolar violations measurements and serves in the generation of a word-sync pulse for each cycle of the test sequence (ref. 4.5.2.4).

4.5.2.4 Receiver Self-Start

Operation and function of this circuit (IC19B) are identical to the Transmitter equivalent. Its input is taken from the Second Zero Counter and its output is routed to the Sequence Generator's 19th stage.

4.5.2.5 Receiver Word Sync

The Word Sync Circuit is a duplicate of its Transmitter counterpart in operation and function. Its input gate (IC7B) is connected to the Second Zero Counter, while its output is directed through inverter IC11E and Q1 to the Display/Count Control (ref. 4.5.3.9) and the Count Interval Control (ref. 4.5.3.7). In the latter circuitry, the word sync pulse serves as the major time base.

4.5.2.6 Receiver Zero Suppression Control

The Receiver Zero Suppression Control circuit operates in a manner similar to its Transmitter counterpart. The Sequence Generator is capable of producing a sequence of up to twenty 0's. To meet the

required pattern specifications, it is necessary to limit 0 sequences to a maximum of fourteen by converting any additional 0's to 1's. IC12A, 16A through D, 7A, and 6 form a zero counter and provide a control signal. The control signal informs the Invert Data Gate (ref. 4.5.2.7) as to which of the output data bits are to be converted from 0's to 1's.

The output of the 20-stage Receiver Sequence Generator is taken from stage 17. The output of stage 1, which occurs sixteen clock periods earlier, is identical to that of stage 17; therefore, stage 1 is a convenient place to count 0's as it provides a preview of the output pattern with sufficient time to detect the presence of more than fourteen sequential 0's before they begin to appear at the Generator's output.

A 4-stage binary counter (IC6) counts Receiver clock pulses when its reset line is at a logical 1. The reset of this counter is connected to the stage 1 output. As long as a 0 is present at this output, the counter is incremented by each clock pulse (1 data bit time), resulting in an indication as to the number of 0's in any one sequence. A gate (IC7A) decodes the counter's outputs for state 15. The output of the decoder is inverted by IC16D which, together with IC16C and B, directs one Receiver clock pulse to the flip-flop (IC12A), which sets it. This set condition informs the Invert Data Gate to begin converting the output data.

To preserve proper timing, a delay of one clock period (one bit) occurs between the fifteenth 0 detected and the setting of the flip-flop. At this point, the contents of the Sequence Generator stages 1 through 16 are 0's. Stage 17 has to be a 1 as it was the last bit before detection of the fifteen-zero sequence. This data bit does not require conversion even though an invert control signal has been generated at this bit time. Here the Receiver deviates from the Transmitter by restricting the Invert Data Gate to a 0-to-1 conversion. The next, and subsequent, shifts of the Generator result in pattern bits of logical 0 weighting. These bits are inverted by the Invert Data Gate. This process continues until the 3rd stage of the Generator contains a 1. As this stage is fourteen bit times before the output, it is used to reset the flip-flop and thus cancel the invert data condition. The next fourteen shifts of the Generator will contain fourteen consecutive 0's, completing the requirement.

4.5.2.7 Invert Data Gate and Comparison Gate

The Invert Data Gate (IC13D) is a NAND gate used for an OR function. Since the Receiver requires only 0-to-1 conversions, an exclusive-OR gate is unnecessary. The output of the Invert Data Gate is not sampled, as in the Transmitter, but is passed directly to the Comparison Gate.

The Comparison Gate (IC19B) is an exclusive-OR used to compare the received data stream from the Bipolar/Unipolar Converter with the test pattern from the Sequence Generator. Comparison is performed bit-by-bit, and any differences appear as logical 1's at the output of the Comparison Gate.

4.5.2.8 Bit Counter

The Bit Counter (IC3, 4, 9A) provides a pulse every twenty bits to the section of Sync Control circuitry (ref. 4.5.2.10) that confirms synchronization. It also provides a narrow pulse every forty bits to the Out-of-Sync Detector (ref. 4.5.2.9).

4.5.2.9 Out-of-Sync Detector

The Out-of-Sync Detector is essentially an error counter which separates incoming data into 40-bit blocks and checks each block for a quantity of errors in excess of twelve; more than twelve errors indicates an out-of-sync condition. The detection process is accomplished by counting logical error pulses from the Error Select circuit (ref. 4.5.3.2) during the 40-bit interval allowed by the reset pulse from the Bit Counter. Counting takes place in IC14A. The gate of IC19C opens for a count of twelve or more to release an out-of-sync pulse to the Sync Control circuit.

4.5.2.10 Sync Control

The Sync Control circuitry opens and closes the Sequence Generator feedback loop and regulates operation of both the NO SYNC and LOST SYNC indicators. Its primary components are IC5A and B, which make up a 2-bit shift register for purposes of sync confirmation. Both stages of the 2-bit register are set under any of the three following conditions: (1) actuation of the RESET/RESYNC switch; (2) receipt of a pulse from the Out-of-Sync Detector; or (3) detection of an error before the shift register can be cleared. The shift register has a logical 0 input and is toggled by the 20-bit output of the Bit Counter (ref. 4.5.2.8); therefore, there must be two consecutive error-free blocks of twenty bits before the register is cleared.

Four gates, at the shift register output, control the NO SYNC indicator and the status of the Sequence Generator loop. If the second stage of the shift register is set, the Receiver is out of sync and the NO SYNC indicator is energized; also, with the VIOLATIONS/ERRORS switch set to VIOLATIONS, the NO SYNC indicator is forced on regardless of sync status. IC15C controls the NO SYNC indicator and the three remaining gates control status of the Loop Control circuit (ref. 4.5.2.2). IC10B allows the shift register to control status of the Sequence Generator's feedback loop only in the AUTO mode; IC15A ORs the automatic sync control with the sync command signal from the RESET/RESYNC switch; IC15B inhibits the Sequence Generator's feedback loop from being opened by any means when the Test Set is set to measure bipolar violations.

For violations measurements, the Sequence Generator is used as a time base only, and it need not be synchronized with the received data since synchronization is achieved by IC15B and the self-start capability of the Generator.

One flip-flop (IC20) and one gate (IC15D) control operation of the LOST SYNC indicator. When sync is regained, the flip-flop is set by IC5A and it energizes the indicator. The flip-flop can be reset only by operating the RESET/RESYNC switch. The gate forces the indicator on when the Test Set is instructed, via the MODE switch, to measure violations.

4.5.3 Receiver Logic Module (A2) (Pages 6-9, 6-10)

4.5.3.1 Violations Sampling and Errors Sampling Flip-Flops

The output of the Comparison Gate (ref. 4.5.2.7) and the output of the Bipolar Violations Detector (ref. 4.5.1.8) are sampled by D-type flip-flops (IC11A and B respectively); thus, detected logical errors and bipolar violations are simultaneously available to the First Errors Selector circuit (ref. 4.5.3.2). These error signals are provided in NRZ format.

4.5.3.2 First Errors Selector

This circuit receives a decision signal from the VIOLATIONS/ERRORS mode switch. The decision signal controls a series of gates (IC10B; 9A, B, C; 4A) which route outputs from either the Violations Sampling or Errors Sampling Flip-Flops (ref. 4.5.3.1) to the input of the Second Errors Selector circuit (ref. 4.5.3.5).

The output of the Errors Sampling Flip-Flop (IC11A) is ANDed with the Receiver clock by IC10B, which converts the sampled output from NRZ to RZ format. The output of this gate is inverted by IC14B, which directs the resulting logical errors signal to the selector gate IC9A, the Out-of-Sync Detector (ref. 4.5.2.9), and the Sync Control (ref. 4.5.2.10). This selector gate routes the logical errors signal to OR gate IC9B when the MODE switch is in the ERRORS position.

In the VIOLATIONS mode, the output of the Violations Sampling Flip-Flop (ref. 4.5.3.1) is ANDed with the Receiver clock (conversion to RZ format) whose output is connected to a second OR gate (IC9B) input. The output of this gate is connected to the Second Errors Selector circuit (ref. 4.5.3.5).

4.5.3.3 1 Hz Oscillator

A 1 Hz source, synchronized to the 1.544 MHz Clock, is provided by IC16 and IC12A, 12B. IC16 is a programmable timer which is connected as a 2 Hz oscillator. IC12B divides the oscillator frequency by two to form a 1 Hz symmetrical signal. This signal is synchronized with the Clock by sampling the 1 Hz at an edge of the clock in IC12A.

4.5.3.4 Block Errors Detector

Block errors detection is accomplished in a 2-stage shift register (IC13A and B). At the first positive edge of the 1 Hz clock signal, a zero

is shifted into IC13A. Any error occurring within the next second will flip IC13A to its 1 state by pulsing its direct preset input via IC14A. At the next positive edge of the 1 Hz clock signal, the state of IC13A is sampled by IC13B and a 0 is shifted into IC13A. Because the 1 Hz clock has been synchronized with the 1.544 MHz Clock, it is impossible for an error pulse to be missed by this circuit, or for two blocks to be in error. Gate IC15C ANDs the output of the Block Errors Detector with one phase of the 1 Hz clock to produce a single 0.5 second pulse for each block in error. This pulse is fed to both the Second Errors Selector (ref. 4.5.3.5) and a test jack drive via inverters IC15B and D.

4.5.3.5 Second Errors Selector

This circuit responds to a command from either of the MODE switches, to select individual errors pulses or block errors pulses for routing to the Errors Gate (ref. 4.5.3.6). Its components are IC14F, 9C, 15A and D, which form a SPDT switch for connection to either violations or errors.

4.5.3.6 Errors Gate

This triple input gate (IC4C) passes an error pulse to the Errors Counter (ref. 4.5.4.1) upon receiving two signals from the Display/Count Control (ref. 4.5.3.8).

4.5.3.7 Count Interval Control

The Count Interval Control consists of two decade counters, (IC1, 2), several gates, and the COUNT INTERVAL (BITS) switch. The counters tally word-sync pulses and provide outputs at one, ten, and one hundred word intervals. The appropriate output is selected via COUNT INTERVAL (BITS) switch positions and selection gates, and it is directed to the Display/Count Control circuit (ref. 4.5.3.9). The counters are reset by the main reset line derived from the Display/Count control. This line also resets the Display Counter. Since a word-sync pulse is generated once per cycle of the test sequence, actual count intervals are determined by multiplying the selected setting of the COUNT INTERVAL (BITS) switch by 1.048,575. Count intervals are based on this quantity because each cycle of the test sequence contains 1,048,575 bits.

4.5.3.8 Display Interval Control

Timing for each display interval is supplied by a programmable unijunction-type oscillator (Q3, 4) with a logic level inhibit and a logic level output. Q1 inhibits operation of the oscillator by shorting timing capacitor C1 during the count interval. Q2 inhibits operation of the oscillator in the ERROR-SECONDS mode, effectively placing the control in HOLD position. Q5 serves as a logic level output buffer. The display interval can be varied

from approximately one to ten seconds by means of the DISPLAY INTERVAL (SEC) potentiometer. Switching this control to HOLD opens the charge path to C1.

4.5.3.9 Display/Count Control

Two flip-flops (IC5A, 7B), with several gates, regulate the gating of errors to the Errors Counter and the resetting of the Counter by synchronizing to the word sync, end-of-count, and end-of-display signals. At the start of each count interval, the word sync pulse, through inverter IC9E, forces flip-flop IC7B to drop the reset line and set count flip-flop IC5A. The count flip-flop, in turn, inhibits the Display Interval Control through Q1, opens errors gate IC4C, and turns on the COUNT indicator. At the end of the count interval, the count flip-flop is reset, reversing the preceding step. The unijunction oscillator then begins to time out unless the DISPLAY INTERVAL (SEC) control is set on HOLD or the Test Set is in the ERROR-SECONDS mode.

At the end of the time-out, flip-flop IC7B sets and causes all counters to reset to 0. They remain reset until the next word sync pulse starts a new count cycle. Each count interval is synchronized to the Sequence Generator by the word sync pulse, as described. Operating the RESET/RESYNC switch at any time will produce the same result as the time-out pulse from the Display Interval Control.

Five additional gates are provided for operation with the COUNT INTERVAL (MIN) mechanical timer. IC6A and B form a flip-flop to debounce the SPDT contacts of the timer. When the timer is in use, IC6C is enabled via IC6D to connect the debounced timer signals to IC3D. This last gate ORs the timer signals with the 10^6 setting of the COUNT INTERVAL (BITS) switch to allow the count interval to terminate on the first word sync pulse following shut-off of the timer.

4.5.4 Display Module (A8) (Pages 6-4, 6-5)

4.5.4.1 Errors Counter

The Errors Counter is a 3-decade arrangement of IC2, 4, 6, and the overflow flip-flop IC7A, located on the Receiver Logic Module (A2). Both the Counter and the overflow flip-flop are reset by the main reset signal from the Display/Count Control.

4.5.4.2 Display

The Display is a 3-digit, solid state type consisting of LED1, 2, 3, with decoder/drivers IC1, 3, 5.

4.5.4.3 Status Display

The Status Display consists of seven light-emitting diodes DS1 through DS7, and their integrated circuit drivers IC7, 8.

4.6 Power Supply Assembly (A6) (Pages 6-2, 6-3)

The Power Supply for the Test Set is composed of transformer T1, capacitor C5, (both chassis mounted), and Power Supply Assembly (A6). The transformer secondary winding is center-tapped and drives a full-wave bridge rectifier composed of diodes CR8 through CR11. This bridge provides plus 12 volts dc (full-wave) and minus 12 volts dc. The plus and minus voltages are filtered by capacitors C5 and C10 respectively. The filtered dc voltages drive positive and negative voltage regulators composed of Q3, Q2, Q1 and Q9, Q8, Q7 respectively. Voltage doubler rectifiers providing plus and minus voltages are composed of C2, CR3, CR4, C4 and C1, CR1, CR2, C3 respectively. These doubler circuits provide approximately ±24 volts to the collector resistors of amplifier transistors Q2, Q8, and Q5.

The +5 volt output regulator uses CR6 as a reference diode, Q2 as an amplifier, and Q1, Q3 as a Darlington pair current driver. The combination of these components acts as a negative feedback amplifier to maintain the output voltage at E6 at +5 Vdc. Components CR13, Q8, Q7, Q9 act in a corresponding fashion as a negative voltage regulator to maintain the output at E8 at -5 Vdc.

An adjustable output voltage regulator is composed of Q5, Q4, Q6, using the -5 Vdc supply as a reference with the output voltage at E7 controlled by potentiometer R6.

5.0 MAINTENANCE

5.1 General

This chapter provides general information required for routine care and maintenance of the Error Rate Test Set. The areas covered include Calibration, Performance Checks, and Troubleshooting Cross-Checks. The Calibration Procedure provides information on all internal adjustments, while Performance Checks are a detailed description and means of measuring the major system waveforms; Troubleshooting Cross-Checks, presented in procedural form, will help to isolate problems to circuit board level where feasible. A Checkout/Self Test Procedure, which provides a quick operational check without the use of external test equipment, is found in Chapter 2.

5.2 Test Equipment Requirements

Recommended test equipment is listed in Table 5-1; equivalent test equipment may be substituted.

5.3 Calibration Procedure

5.3.1 Preliminary

a. With the POWER switch at OFF, remove the power cable from the Test Set.

b. Remove the four screws from the rear of the carrying case and slide the Test Set out.

c. Reconnect the power cable and set the POWER switch at ON.

> WARNING
> Voltages as high as 115 volts will be present in the vicinity of the POWER switch, fuseholders, and power input.

d. Connect the Test Set only to equipment as directed below.

Table 5-1: Test Equipment Required

EQUIPMENT TYPE	REQUIRED CHARACTERISTICS	USE (REF. PAR.)	RECOMMENDED MODEL
Frequency Counter	Measurement: frequency, period. Frequency Range: 10 MHZ with a 1 Hz resolution.	5.3.2 5.3.8 5.4.1.1	General Radio 1191
Oscilloscope	50 MHz dual time base.	5.3.3 5.3.4 5.3.5 5.4.1.2 5.4.2.2 5.5.3	Tektronix 547
Storage Oscilloscope	30 MHz	5.4.1.3 5.4.2.2 5.5.3	Tektronix 549
Oscilloscope Plug-In			Tektronix 1A1
DC Power Supply	Voltage Range: 10 V at 500 mA	5.4.1.3 5.4.2.1 5.5.3	Power Designs TW5005
Digital DC Voltmeter	3-1/2 Digit	5.3.7	Fluke 8000A
Test Transmitter	Pattern: selection of 7. a. ALL 1'S b. 1 and seven 0's, alternating c. 1 and nine 0's, alternating d. 1 and eleven 0's, alternating e. 1 and thirteen 0's, alternating f. 1 and fifteen 0's, alternating g. 1 and seventeen 0's, alternating Waveform: 1.544 Mbps, 3 V peak, bipolar, return-to-zero.	5.4.2.1	Bowmar/ALI D271-129
Test Receiver	Convert bipolar return-to-zero pattern to unipolar pattern.	5.4.1.3 5.5.3	Bowmar/ALI D271-130
Standard Error Rate Test Set	Qualified for use as an operating standard by: (1) successfully passing Self Test requirements, par.2.2 of this manual, (2) being certified as synchronized to a Western Electric J98710R T1 Quasi-Random Signal Source without recording errors, and (3) being certified to insert and detect both errors and violations, exclusive of one another.	5.4.1.3 5.5.3 5.5.4	Bowmar/ALI Model 271A or 271B
BNC to BNC Coaxial Cable		5.3.5	
Patch Cord	WE 310-type plug at each end.		
T1 Quasi-Random Signal Source	Pattern: 1,048,575 bit quasi-random, restrained to a maximum of fourteen consecutive 0's. Waveform: 1.544 Mbps, 3 V peak, bipolar, return-to-zero signal.	5.4.1.3 5.4.2.1 5.5.3 5.5.4	Western Electric J98710R
100 Ohm Resistor	Accuracy: 1% Alligator clips at each end.	5.4.2.2 5.5.3	
Tapped Termination (1)		5.3.3 5.4.1.2 5.5.3	See Figure 5-1
Cable Simulator (1)		5.4.2.1	See Figure 5-2
24 dB Attenuator (1)		5.4.2.1	See Figure 5-3
Termination (3)		5.4.1.2	See Figure 5-4

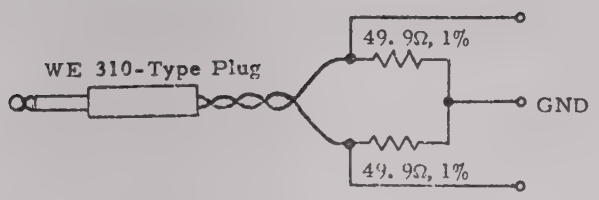


Figure 5-1: Tapped Termination

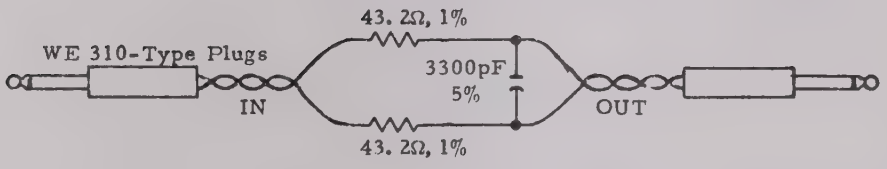


Figure 5-2: Cable Simulator

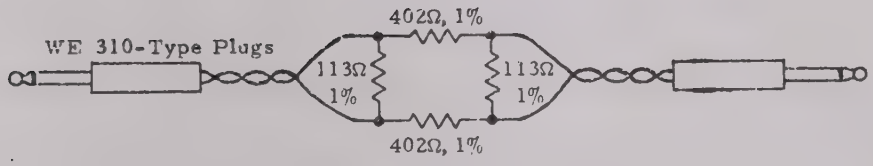


Figure 5-3: 24 dB Attenuator

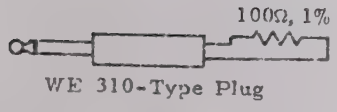


Figure 5-4: Termination

5.3.2 Transmitter Oscillator Frequency Adjustment

(To be made only after a 1-hour minimum warm-up of the unit under test.)

a. Connect the Frequency Counter to the TRANSMITTER BIT SYNC and GND.

b. Adjust the Frequency Counter for a 1-second count.

c. Adjust capacitor C3, at the rear edge of the Transmitter Module (A5) for a frequency of 1,544,000 ±5 Hz.

d. Disconnect the Frequency Counter.

5.3.3 Transmitter Amplitude Adjustment

a. Set up the Oscilloscope as follows.

	HORIZONTAL DISPLAY	A
	SWEEP MAGNIFIER	X1 OFF
TIME BASE A:	TIME/CM	.1 μSEC
	TRIGGERING:	
	MODE	TRIG
	SLOPE	+
	COUPLING	AC LF REJ
	SOURCE	INT
1A1 Plug-In:	MODE	CH1
	INPUT SELECTOR	DC
	VOLTS/CM	.05

b. Plug the Tapped Termination into any one of the Test Set DS1 OUTPUT jacks.

c. Connect an X10 Probe to the Tapped Termination GND and either of its outer taps.

d. Adjust potentiometer R6 (+5V Adjust) on the Power Supply Assembly (A6) for a pulse height of 3 cm (1.5 V) peak or 6 cm (3.0 V) peak-to-peak, as shown in Figure 5-5.

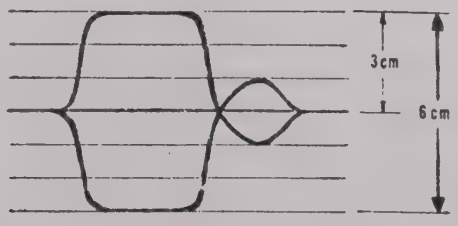


Figure 5-5: Transmitter Amplitude

e. Disconnect test equipment from the Test Set.

5.3.4 Clock Extractor Tuning Adjustment

a. Set up the Oscilloscope as follows.

	HORIZONTAL DISPLAY	A
	SWEEP MAGNIFIER	X1 OFF
TIME BASE A:	TIME/CM	.1 μSEC
	TRIGGERING:	
	MODE	TRIG
	SLOPE	— (negative)
	COUPLING	AC LF REJ
	SOURCE	EXT
1A1 Plug-In:	MODE	CH1
	INPUT SELECTOR	DC
	VOLTS/CM	.1

b. Using an X1 Probe, connect the Test Set TRANSMITTER BIT SYNC output to the TRIGGER INPUT of the Oscilloscope; connect the Probe ground lead to the Test Set GND terminal.

c. Using an X10 Probe, connect the Test Set RECEIVER BIT SYNC output to the Plug-In CHANNEL 1 INPUT; connect the Probe ground lead to the Test Set GND terminal.

d. Use a tuning tool to adjust inductor L1 on the Receiver Module (A4) for a symmetrical source wave with clean transitions.

e. Switch the SWEEP MAGNIFIER to X10 and adjust the Oscilloscope position controls to bring a transition into view. (See Figure 5-6).

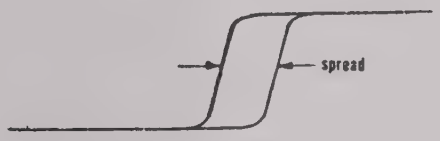


Figure 5-6: Transition Adjustment

f. Continue to adjust L1 for minimum spread on the transition edge, using the Oscilloscope position controls to keep the pattern centered or conveniently located.

g. After adjustment, lock the tuning slug of L1 with coil wax.

h. Remove the Probes from the Test Set and Oscilloscope.

5.3.5 Clock Extractor Phase Adjustment

a. Set up the Oscilloscope as follows.

	HORIZONTAL DISPLAY	A
	SWEEP MAGNIFIER	X5
TIME BASE A:	TIME/CM	.1 μSEC
	TRIGGERING:	
	MODE	TRIG
	SLOPE	— (negative)
	COUPLING	AC LF REJ
	SOURCE	EXT
1A1 Plug-In:	MODE	ALTERNATE
	INPUT SELECTOR	DC
	VOLTS/CM	.2

b. Connect the BNC to BNC Coaxial Cable between the SIGNAL OUT jack of the Plug-In and the TRIGGER INPUT of TIME BASE A.

c. Using an X10 Probe, connect the Plug-In CHANNEL 1 INPUT and TP3 of the Receiver Module (A4). Using a second X10 Probe, connect the Plug-In CHANNEL 2 INPUT and TP2 of the Receiver Module.

d. Adjust the Oscilloscope position controls and VARIABLE TIME/CM vernier to obtain the pattern of Figure 5-7, with the upper trace symmetrically positioned.

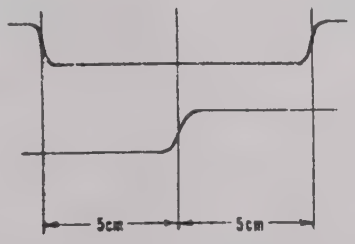


Figure 5-7: Clock Extractor Phase Adjustment

e. Adjust capacitor C11 on the Receiver Module to position the lower trace at the center of the upper trace.

f. Disconnect the test equipment from the Test Set.

5.3.6 No Data Threshold Adjustment

a. Holding the SELF TEST switch of the Test Set at INTERRUPT DATA, observe the NO DATA indicator.

b. If the indicator is off, proceed to the next step. If the indicator is on,

adjust potentiometer R56 on the Receiver Module (A4) clockwise until the NO DATA indicator goes off, and then proceed to the next step.

c. Slowly adjust potentiometer R56 counterclockwise until the NO DATA indicator comes on. Continue adjusting the potentiometer three full turns past this point. Release the SELF TEST switch.

d. Check the operation of the NO DATA indicator by momentarily operating the SELF TEST switch to INTERRUPT DATA and releasing it to NORMAL.

5.3.7 Lost Power Threshold Adjustment

a. Switch the Test Set power to OFF.

b. Remove the Receiver Module (A4) from the Test Set and remove the jumper attached to test point TP5.

c. Attach the Digital DC Voltmeter negative lead to TP5 and its positive lead to the +5V Test Terminal on the Power Supply Assembly (A6), accessible through a hole in the side plate.

d. Carefully replace the Receiver Module and switch the Test Set power to ON.

e. Adjust potentiometer R61 on the Receiver Module for a reading of 3.80 V dc.

f. Switch the Test Set power to OFF and remove the Receiver Module.

g. Disconnect the Voltmeter and replace the jumper at TP5.

h. Replace the Receiver Module.

5.3.8 1 Hz Oscillator Adjustment

a. With the Test Set power OFF, remove the Receiver Reference Module (A1).

b. Connect the Frequency Counter to test point TP1 of the Receiver Logic Module (A2). (It may be necessary to temporarily remove the Receiver Logic Module for this connection.)

c. Switch the Test Set power to ON. Adjust the Frequency Counter to perform a period measurement on one cycle of its input.

d. Slowly adjust potentiometer R14 on the Receiver Logic Module for a period of 1,000 msec on the Frequency Counter. **

e. Switch the Test Set power to OFF and remove the Frequency Counter connections.

f. Replace the Receiver Reference Module in the chassis.

*Note: If the oscillator does not oscillate, adjust the potentiometer R14 counter-clockwise until oscillation begins. Then resume Step d above.

5.3.9 Final

a. Return the Test Set to its case and secure with the four screws to the rear panel.

b. Perform the Checkout/Self Test of section 2.2.

5.4 Performance Checks

Performance checks are made with the Test Set in its case unless otherwise directed. They serve as checks for periodic maintenance, quality control, and post-repair. They also serve as a check when a malfunction is suspected.

5.4.1 Transmitter Checks

5.4.1.1 Clock Frequency Check

a. Allow the Test Set to temperature stabilize by operating continuously for at least one hour at room temperature.

b. Connect the Frequency Counter input to the Test Set TRANSMITTER BIT SYNC output and GND terminal.

c. Adjust the Frequency Counter for a 1-second count interval (to read directly in Hertz), and adjust the Counter input controls for a consistent display. The Counter should register between 1,543,950 and 1,544,050 Hz at the end of each count interval.

d. Disconnect the Frequency Counter.

5.4.1.2 Bipolar Output Check

a. Set up the Oscilloscope as follows.

	HORIZONTAL DISPLAY	A
	SWEEP MAGNIFIER	X1 OFF
TIME BASE A:	TIME/CM	.1 μSEC
	TRIGGERING:	
	MODE	TRIG
	SLOPE	— (negative)
	COUPLING	AC LF NEG
	SOURCE	EXT
1A1 Plug-In:	MODE	CH 1
	INPUT SELECTOR	DC
	VOLTS/CM	.05

b. Insert the Tapped Termination plug into the first (top) DS1 OUTPUT jack of the Test Set, and insert the three Terminations into the remaining jacks. Connect an X10 Probe to the Tapped Termination GND and either of its outer taps.

c. Adjust the Oscilloscope trigger, intensity, and position controls to obtain the waveform shown in Figure 5-8.

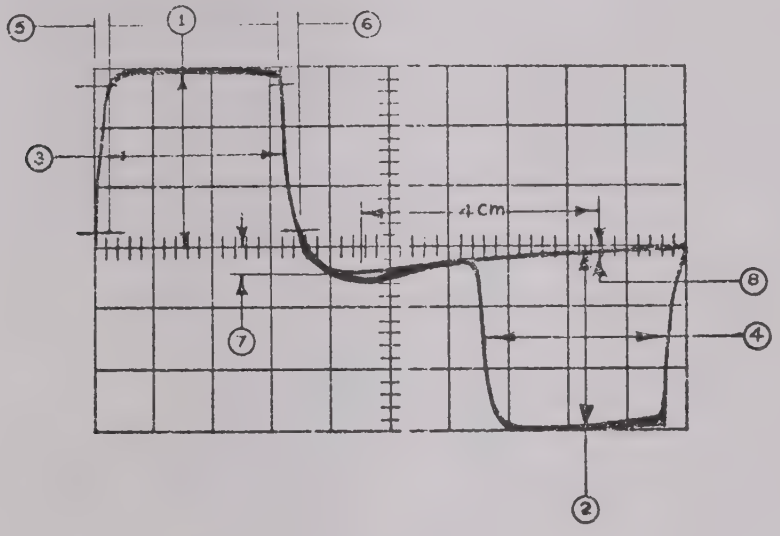


Figure 5-8: Bipolar Waveform

d. The measurements designated ① and ② in Figure 5-8 should be between 2.7 and 3.3 cm (1.35 and 1.65 volts). Resultant measurements should differ by not more than 0.15 cm (0.075 volts).

e. Measurements ③ and ④ should be between 3.0 and 3.5 cm (300 and 350 nsec). Resultant measurements should differ by not more than 0.15 cm (15 nsec).

f. Measurements ⑤ and ⑥, taken between 10% and 90% of peak points, should be less than 0.8 cm (80 nsec).

g. Measurement ⑦ should be between 10% and 30% of the base line to peak reading (nominally 0.3 and 0.9 cm for a 3.0 cm peak).

h. Measurement ⑧, taken 4.0 cm to the right of the point of measurement ⑦, should be less than 10% of measurement ⑦. (It may be necessary to increase the vertical sensitivity in order to make this measurement.)

i. Exchange positions of the Tapped Termination and the Termination in the second DS1 OUTPUT jack. Repeat steps d through h.

j. Exchange positions of the Tapped Termination and the Termination in the third DS1 OUTPUT jack. Repeat steps d through h.

k. Exchange positions of the Tapped Termination and the Termination in the fourth (bottom) DS1 OUTPUT jack. Repeat steps d through h.

l. One at a time, remove the three Terminations and observe the Oscilloscope trace. The trace should not be altered as the terminations are removed. Finally, move the Tapped Termination to any one of the other three DS1 OUTPUT jacks. The waveform of Figure 5-8 should reappear on the Oscilloscope.

m. Momentarily operate the SELF TEST switch to both INTERRUPT DATA and INSERT ERRORS while observing the Oscilloscope. The waveform should remain unchanged.

n. Remove all test equipment from the Test Set.

5.4.1.3 Pattern Content and Error Insertion Check

a. Connect the Patch Cord between any one of the DS1 OUTPUT jacks of the Test Set under check and the DS1 INPUT jack of the Standard Test Set.

b. Set the Standard Test Set controls as follows.

MODE	
VIOLATIONS/ERRORS	- to ERRORS
INDIVIDUAL/ERROR-SECONDS	- to INDIVIDUAL (271B)
SYNC MODE	- to AUTO
SELF TEST	- to NORMAL
DISPLAY INTERVAL (SEC)	- to '1' (full ccw)
COUNT INTERVAL (BITS)	- to '10^6'
COUNT INTERVAL (MIN)	- to '0' (271B)

c. The Standard Test Set NO DATA and NO SYNC indicators should be off, and its Display should continuously read '00' ('000').

d. Set the VIOLATIONS/ERRORS switch of the Test Set under check to ERRORS, and hold its SELF TEST switch at INSERT ERRORS. The Display of the Standard Test Set should count to a final reading of '08' ('008') at the end of each full-count interval. (To the eye, the Display will appear to count by increments of two.)

e. Set the VIOLATIONS/ERRORS switch of the Test Set under check to VIOLATIONS, and continue holding its SELF TEST switch at INSERT ERRORS. The Standard Test Set Display should clear to and remain at '00' ('000').

f. Set the Standard Test Set VIOLATIONS/ERRORS switch to VIOLATIONS and continue holding the SELF TEST switch of the Test Set under check at INSERT ERRORS. The Standard Test Set Display should count to a final reading of '08' ('008') at the end of each full-count interval.

g. Set the VIOLATIONS/ERRORS switch of the Test Set under check to ERRORS, and continue holding its SELF TEST switch at INSERT ERRORS. The Standard Test Set Display should clear to and remain at '00' ('000').

h. Release the SELF TEST switch. Remove the Patch Cord.

i. ✓ Set the controls of the Storage Oscilloscope as follows.

	UPPER SCREEN STORAGE	STORE
	LOWER SCREEN STORAGE	STORE
	SCREEN SELECTOR	FULL
	AUTO ERASE	OFF
Time Base A:	TIME/CM	2 μSEC
	HORIZONTAL DISPLAY	A, SINGLE SWEEP
	MAGNIFIER	OFF
	TRIGGERING:	
	MODE	TRIG
	SLOPE	— (negative)
	COUPLING	AC LF REJ
	SOURCE	EXT
1A1 Plug-In:	MODE	CH 1
	INPUT SELECTOR	DC
	VOLTS/CM	.1

j. Connect an X1 Probe to the TRIG INPUT jack of the Storage Oscilloscope. Insert the Probe tip into the Test Set TRANSMITTER WORD SYNC jack, and attach the Probe ground lead to the Test Set GND terminal.

k. ✓ Connect the DC Power Supply to the Test Receiver. Connect the Patch Cord between the Test Receiver SIGNAL IN jack and any DS1 OUTPUT jack.

l. Connect an X10 Probe to the Test Receiver OUTPUT and GND terminals.

m. Operate the Storage Oscilloscope LEVEL/STABILITY controls and its ERASE AND RESET pushbutton to obtain the waveform of Figure 5-9. The waveform should appear each time the pushbutton is operated. Observe the waveform carefully - it should contain fourteen time slots in which there are no pulses. Measurement ①, measured from the beginning of the trace, should be between 0.3 and 0.5 cm (600 and 1000 nsec).

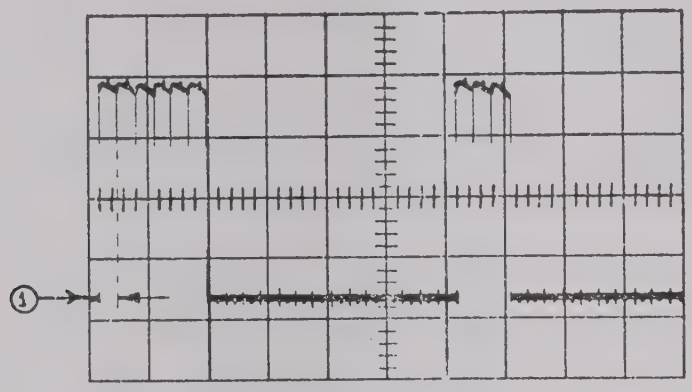


Figure 5-9: Typical 14-Zero Condition with No Errors

n. Hold the Test Set SELF TEST switch at INSERT ERRORS and operate the Storage Oscilloscope ERASE/RESET pushbutton. The waveform should now appear as in Figure 5-10, containing only thirteen time slots with no pulses. Measurement ①, as measured from the beginning of the trace, should be between 0.3 and 0.5 cm (600 and 1000 nsec).

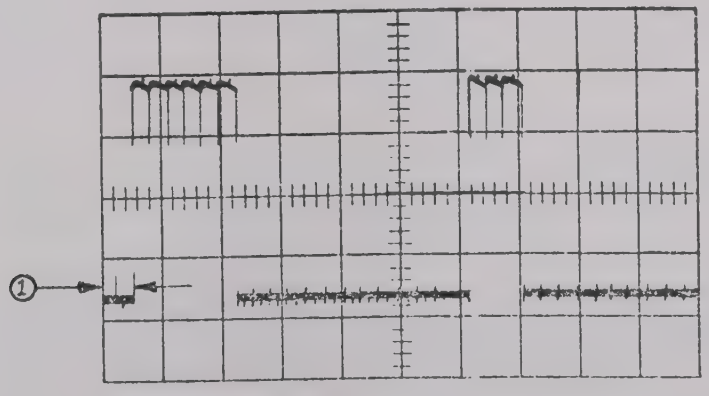


Figure 5-10: Typical 13-Zero Condition with Two Errors

o. Disconnect all test equipment.

5.4.2 Receiver Checks

Be sure that all switches of the Test Set are at the following positions before performing any of the Receiver Checks.

MODE	
VIOLATIONS/ERRORS	- to VIOLATIONS
INDIVIDUAL/ERROR-SECONDS	- to ERROR-SECONDS
SYNC MODE	- to MANUAL
SELF TEST	- to NORMAL
DISPLAY INTERVAL (SEC)	- to '1' (full ccw)
COUNT INTERVAL (BITS)	- to '10^6'
COUNT INTERVAL (MIN)	- to '0'
RESET/RESYNC	- momentarily actuate and release

5.4.2.1 Receiver Sensitivity to Level and Data Content Check

a. Insert the Cable Simulator IN plug into one of the Test Set DS1 OUTPUT jacks, and the OUT plug into the DS1 INPUT jack. The NO DATA indicator should be off, and the Display should read '000' at all times.

b. Remove the Cable Simulator and replace it with the 24 dB Attentuator. The NO DATA indicator should be off, and the Display should read '000' at all times.

c. Hold the Test Set SELF TEST switch at INTERRUPT DATA; the NO DATA indicator should remain off.

d. Release the SELF TEST switch and remove the 24 dB Attenuator. Connect the DC Power Supply to the Test Transmitter. Connect the Patch Cord between the Test Transmitter OUTPUT jack and the Test Set DS1 INPUT jack.

e. Set the Test Transmitter PATTERN switch at '16'; momentarily operate the RESET pushbutton. The Test Transmitter should provide a bipolar pattern of a single 1 followed by fifteen 0's.

f. Press and hold the Test Transmitter RESET pushbutton. The Test Set NO DATA indicator should illuminate immediately.

g. Release the RESET pushbutton. The NO DATA indicator should go off and the Display should read '000' at all times.

h. Replace the Patch Cord with the 24dB Attenuator and repeat Steps e, f, g.

i. Remove all test equipment.

5.4.2.2 Auxiliary Output Checks

a. Set the Oscilloscope controls as follows.

	HORIZONTAL DISPLAY	A
	SWEEP MAGNIFIER	X1 OFF
TIME BASE A:	TIME/CM	.1 μSEC
	TRIGGERING:	
	MODE	TRIG
	SLOPE	— (negative)
	COUPLING	DC
	SOURCE	NORM
1A1 Plug-In:	MODE	CH 1
	INPUT SELECTOR	DC
	VOLTS/CM	.1

b. Connect the ground lead of an X10 Probe to the Test Set GND terminal, and insert the Probe tip into the Test Set TRANSMITTER BIT SYNC jack.

c. Adjust the Oscilloscope trigger level and position controls for the waveform of Figure 5-11. Measurement ① should be between 4.5 and 5.5 cm (4.5 and 5.5 volts). Measurement ② should be between 3.0 and 3.5 cm (300 and 350 nsec). Measurements ③ and ④, taken at the 10% and 90% points, should be less than 0.5 cm (50 nsec).

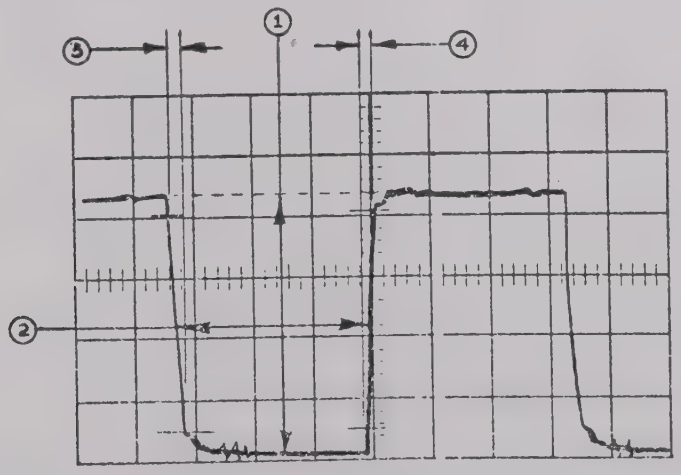


Figure 5-11: BIT SYNC Waveform

d. Fasten the 100 Ohm Resistor between the Probe tip and the Test Set GND terminal. Measurement ① of Figure 5-11 should now be between 2.25 and 2.75 cm (2.25 and 2.75 volts).

e. Remove the Resistor. Move the Probe tip to the RECEIVER BIT SYNC jack. Repeat steps c and d.

f. Remove the Resistor. Move the Probe tip to the ERRORS jack. Momentarily push the SELF TEST switch to INTERRUPT DATA so as to force the Receiver out of synchronization and thereby produce a large number of errors.

g. Observe the waveform of Figure 5-12. Measurement ① should be between 4.5 and 5.5 cm (4.5 and 5.5 volts). Measurement ② should be between 3.0 and 3.5 cm (300 and 350 nsec). Measurements ③ and ④, taken at the 10% and 90% points, should be less than 0.5 cm (50 nsec).

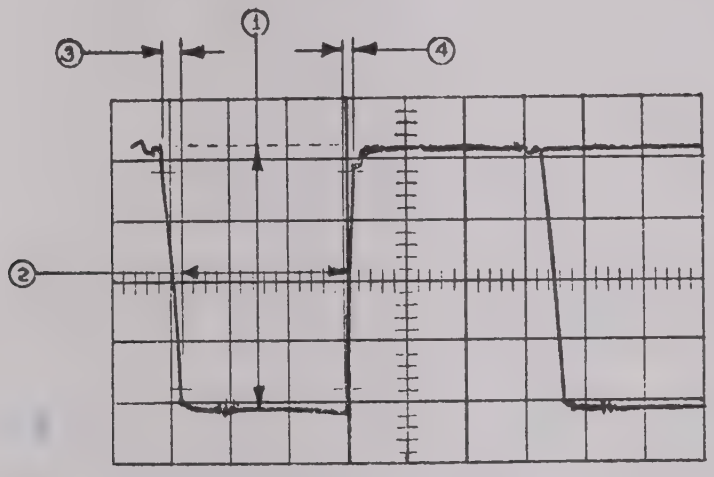


Figure 5-12: ERRORS Waveform

h. Fasten the 100 Ohm Resistor between the Probe tip and the Test Set GND terminal. Measurement ① of Figure 5-12 should now be between 2.25 and 2.75 cm (2.25 and 2.75 volts).

i. Remove the Resistor. Move the Probe tip to the ERROR-SECONDS jack.

j. Adjust the Oscilloscope trigger level and position controls to obtain the waveform shown in Figure 5-13. Measurement ① should be between 4.5 and 5.5 cm (4.5 and 5.5 volts). Measurement ② should be between 4.75 and 5.25 cm (475 and 525 msec). Measurement ③ should be between 9.50 and 10.50 cm (950 msec and 1.05 sec).

k. Fasten the 100 Ohm Resistor between the Probe tip and the Test Set GND. Measurement ① of Figure 5-13 should now be between 2.25 and 2.75 cm (2.25 and 2.75 volts).

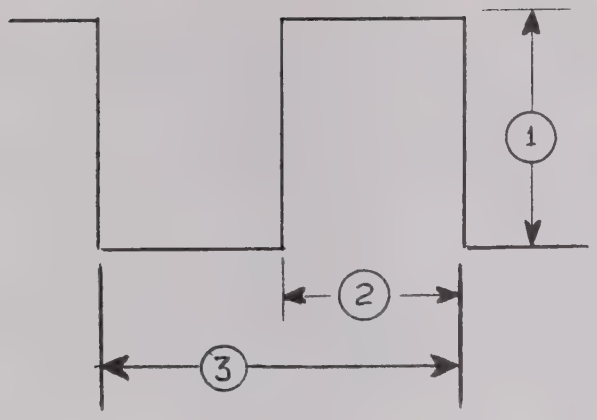


Figure 5-13: ERROR-SECONDS Waveform

l. Remove the test equipment from the Test Set.

m. Set up the Storage Oscilloscope as follows.

	UPPER SCREEN STORAGE	STORE
	LOWER SCREEN STORAGE	STORE
	SCREEN SELECTOR	FULL
Time Base A:	TIME/CM	.1μSEC
	HORIZONTAL DISPLAY	A, SINGLE SWEEP
	MAGNIFIER	OFF
	TRIGGERING:	
	MODE	TRIG
	SLOPE	— (negative)
	COUPLING	AC LF REJ
	SOURCE	NORM
1A1 Plug-In:	MODE	CH 1
	INPUT SELECTOR	DC
	VOLTS/CM	.1

n. Connect the ground lead of an X10 Probe to the Test Set GND terminal, and insert the Probe tip into the Test Set TRANSMITTER WORD SYNC jack.

o. Operate the Oscilloscope LEVEL/STABILITY controls with its ERASE AND RESET pushbutton to obtain the waveform of Figure 5-14. Measurement ① should be between 4.5 and 5.5 cm (4.5 and 5.5 volts). Measurement ② should be between 3.0 and 3.5 cm (300 and 350 nsec). Measurements ③ and ④, taken at the 10% and 90% points, should be less than 0.5 cm (50 nsec).

p. Connect the 100 Ohm Resistor between the Probe tip and the Test Set GND terminal. Measurement ① of Figure 5-14 should be between 2.25 and 2.75 cm (2.25 and 2.75 volts).

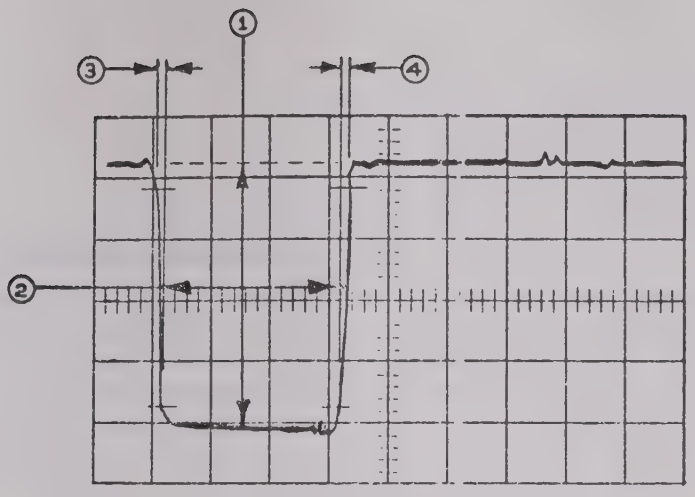


Figure 5-14: WORD SYNC Waveform

q. Remove the Resistor. Move the Probe to the RECEIVER WORD SYNC jack. Repeat steps o and p.

r. Change the Storage Oscilloscope TRIGGERING SOURCE control to EXT. Move the X10 Probe tip to the TRANSMITTER BIT SYNC jack. Connect an X1 Probe to the TRIG INPUT jack of the Oscilloscope; connect the X1 Probe ground lead to the Test Set GND terminal and insert its tip into the TRANSMITTER WORD SYNC jack.

s. Adjust the Oscilloscope trigger level and position controls to obtain the waveform of Figure 5-15. When properly triggered, the Oscilloscope should exhibit a slight delay (not more than 2/3 second) between release of the ERASE AND RESET pushbutton and the actual sweep. Measurement (1) should be between 1 and 3 cm (100 and 300 nsec) from the beginning of the trace.

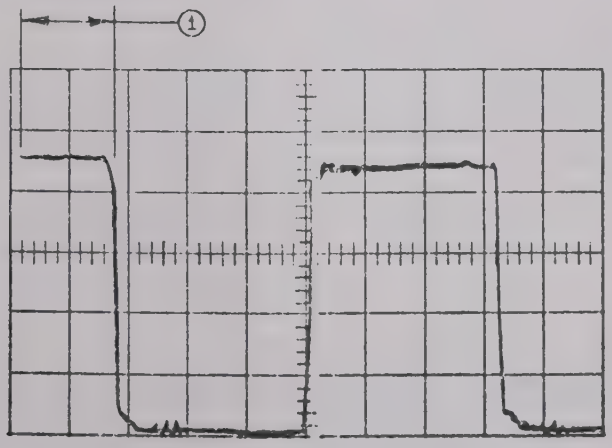


Figure 5-15: BIT SYNC Waveform

t. Disconnect all test equipment from the Test Set.

5.4.2.3 Timer Check

Set the Count Interval to 120 minutes and measure the time that the timer runs the Test Set. The time should be 120 ± 10 minutes. Set the Count Interval to 60 minutes and measure the time that the timer runs the Test Set. The time should be 60 ± 11 minutes.

5.5 Troubleshooting Cross-Checks

5.5.1 Preliminary

Unless otherwise specified, the following procedures are to be performed with the Test Set in its case. Their intent is to aid in isolating the cause of malfunction to at least circuit board level. In some cases, more than one procedure can be used to isolate a problem; the choice may be dictated by availability of test equipment. Before proceeding, connect the Test Set to a power source of 115 V ac ±10%, 50 to 60 Hz. The Test Set's fuse should have been checked, and replaced if necessary.

WARNING

If the Test Set is removed from its case, voltages as high as 115 volts will be present in the vicinity of the POWER switch, fuseholders, and power input.

Connect equipment to the Test Set only as directed below.

5.5.2 Power Supply

a. A Power Supply malfunction may be suspected if any of the following conditions exist:

(1) The Test Set repeatedly blows fuses of the proper size and type (Littelfuse 3 AG, 1/2 A, Slo Blo).

(2) The Display and solid state indicators are too bright, too dark, or off while the power indicator remains illuminated.

(3) The Transmitter and Receiver simultaneously fail tests outlined in the sections that follow.

b. A suspected Power Supply malfunction can be confirmed by removing the Test Set from its case and checking the three test points, visible through an opening in the right side plate, with a DC Voltmeter. Voltages at the test points should be within the ranges specified below:

Test Point	Voltage Range
+5	+4.5 to +5.5 Vdc
-5	-4.5 to -5.5 Vdc
+5 ADJ	+4.0 to +6.0 Vdc

If a short circuit appears likely, remove the plug-in modules, one at a time, while monitoring the shorted supply point. This action should narrow isolation of the short to one of the boards or to the chassis wiring. If the voltages measured above are not within specified limits, the modules should be removed from the Test Set until repairs are complete.

5.5.3 Transmitter

a. Perform the Pattern Content and Error Insertion Checks, steps a through h (ref. 5.4.1.3). Any failure indicated by these checks may be attributed to the Transmitter Module (A5).

b. The Transmitter can be further analyzed by comparing its bipolar waveform with that shown in Figure 5-8 (ref. 5.4.1.2, Bipolar Output Checks).

5.5.4 Receiver

a. Connect the Patch Cord between the DS1 INPUT jack of the Test Set under check and any one of the DS1 OUTPUT jacks of the Standard Test Set.

b. Set switches to the following initial positions.

	Test Set Under Check	Standard Test Set
MODE		
VIOLATIONS/ERRORS	VIOLATIONS	VIOLATIONS
INDIVIDUAL/ERROR-SECONDS	INDIVIDUAL	INDIVIDUAL (271B)
SYNC MODE	MANUAL	AUTO
SELF TEST	NORMAL	NORMAL
DISPLAY INTERVAL (SEC)	'10^6'	'10^6'
COUNT INTERVAL (BITS)	'1' (full ccw)	'1' (full ccw)

c. On the Test Set under check, the initial response of indicators should be as follows.

NO DATA	- off (after momentarily operating the RESET/RESYNC switch)
LOST DATA	- off
NO SYNC	- on
LOST SYNC	- on
LOST POWER	- off
OVERFLOW	- off
COUNT	- alternately on for approximately 2/3 second, off for approximately 1 second
Display	- '000'

d. If the Test Set under check passes the Checkout/Self Test (ref. 2.2) but fails step c above, or vice versa, the malfunction may be located in the Receiver Module (A4), in the connection between the input jack and the Module, or in the SELF TEST switch.

e. If the NO DATA indicator remains on and the COUNT indicator remains either on or off while signal is being supplied to the input jack, the malfunction is most likely in either the Receiver Module (A4) or the connection between the input jack and the module.

f. If the LOST DATA or LOST POWER indicators remain on after momentarily operating the RESET/RESYNC switch, the malfunction is most likely in the Receiver Module (A4), in the RESET/RESYNC switch, or in connections between the switch and module.

g. If the COUNT indicator remains off, momentarily operate the RESET/RESYNC switch of the Test Set under check. If the COUNT indicator comes on within 2/3 second of the release of this switch, the malfunction is most likely in the DISPLAY INTERVAL (SEC) control, the connections between the control and the Receiver Logic Module (A2), or the discrete circuitry on the module.

h. If the COUNT indicator comes on as described in the preceding step but fails to go off after 2/3 second, the malfunction is most likely in the Count Interval Control circuit on the Receiver Logic Module (A2) or in the wiring between the COUNT INTERVAL (BITS) switch and the module.

i. If the COUNT indicator fails to come on in step g above, and:

(1) If the RECEIVER BIT SYNC signal fails to appear as described in 5.4.2.2, step e, the malfunction is most likely in the Clock Extractor circuit or the No Data Detector circuit on the Receiver Module (A4).

(2) If the RECEIVER BIT SYNC signal appears as described, but the RECEIVER WORD SYNC signal fails to appear, as described in 5.4.2.2, step q, the malfunction is most likely in the Receiver Reference Module (A1).

(3) If both signals appear as described, the malfunction is most likely located in the Count Interval Control circuit on the Receiver Logic Module (A2).

j. Assuming that the NO DATA indicator is off and the COUNT indicator is operating properly, hold the SELF TEST switch of the Standard Test Set in the INSERT ERRORS position. The indicated count on the Display of the Test Set under check should clear to a starting count of '000' and progress to a final count of '008' while the COUNT indicator is on. During the counting process, the spacing of errors will

cause the Display to appear to be counting by increments of two. At the count of '008', the Display will hold for the period set by the DISPLAY INTERVAL (SEC) control, then clear to '000' and begin a new cycle.

k. If the Display of the Test Set under check appears to be counting correctly, but one or more segments are missing from the Display, the malfunction is located on the Display Module (A8).

l. Change the VIOLATIONS/ERRORS switches of both the Test Set under check and the Standard Test Set to ERRORS position and momentarily operate the RESET/RESYNC switch of the Test Set under check. Repeat step j above.

(1) If the Display of the Test Set under check fails to count properly in both VIOLATIONS and ERRORS modes, the problem is most likely located in the Receiver Logic Module (A2) or the Display Module (A8).

(2) If the Display operates properly in the ERRORS mode but not in the VIOLATIONS mode, the problem is most likely located on the Receiver Module (A4).

(3) If the Display operates properly in the VIOLATIONS mode but not in the ERRORS mode, or the NO SYNC or LOST SYNC indicators are on, the malfunction is likely to be on the Receiver Reference Module (A1).

NOTE: An out-of-sync condition is indicated by illumination of the NO SYNC indicator and a Display reading of '888', with an OVERFLOW indication during the count interval and any number with an OVERFLOW indication at the end of the count interval.

m. Failure during any of the next three checks, after having successfully completed step j, indicates a problem most likely to be located in the Count Interval Control circuit on the Receiver Logic Module (A2), in the COUNT INTERVAL (BITS) switch, or in the wiring between the module and switch.

(1) Change the COUNT INTERVAL (BITS) switch of the Test Set under check from 10^6 to 10^7, and continue holding the SELF TEST switch of the Standard Test Set at INSERT ERRORS position. The Display should perform as in step j above to a final count of '080' per count cycle.

(2) Change the COUNT INTERVAL (BITS) switch of the Test Set under check from 10^7 to 10^8, and continue holding the SELF TEST switch of the Standard Test Set at INSERT ERRORS position. The Display should perform as in step j above to a final count of '800' per count cycle.

(3) Change the COUNT INTERVAL (BITS) switch of the Test Set under check from 10^8 to CONT, and continue holding the SELF TEST switch

of the Standard Test Set at INSERT ERRORS position. The Display should clear to '000' and then count continuously by increments of two; the OVERFLOW indicator should come on as the Display overflows from '998' to '000'. The Test Set should be checked in this manner for at least 90 seconds.

n. Release the SELF TEST switch of the Standard Test Set and return the COUNT INTERVAL (BITS) switch of the Test Set under check to its 10^6 position.

o. Failure during any of the next three checks would indicate a problem most likely to be located on the Receiver Reference Module (A1).

(1) Set the SYNC MODE switch of the Test Set under check to AUTO and remove the Patch Cord from the DS1 INPUT jack of the Standard Test Set. The NO DATA and NO SYNC indicators should come on immediately; the LOST DATA and LOST SYNC indicators may or may not come on.

(2) Reconnect the Patch Cord to the DS1 INPUT jack of the Standard Test Set. The NO DATA and NO SYNC indicators should go off; the LOST DATA and LOST SYNC indicators should come on if not already on.

(3) Momentarily operate the RESET/RESYNC switch. The NO DATA and NO SYNC indicators should remain off and the LOST DATA and LOST SYNC indicators should go off.

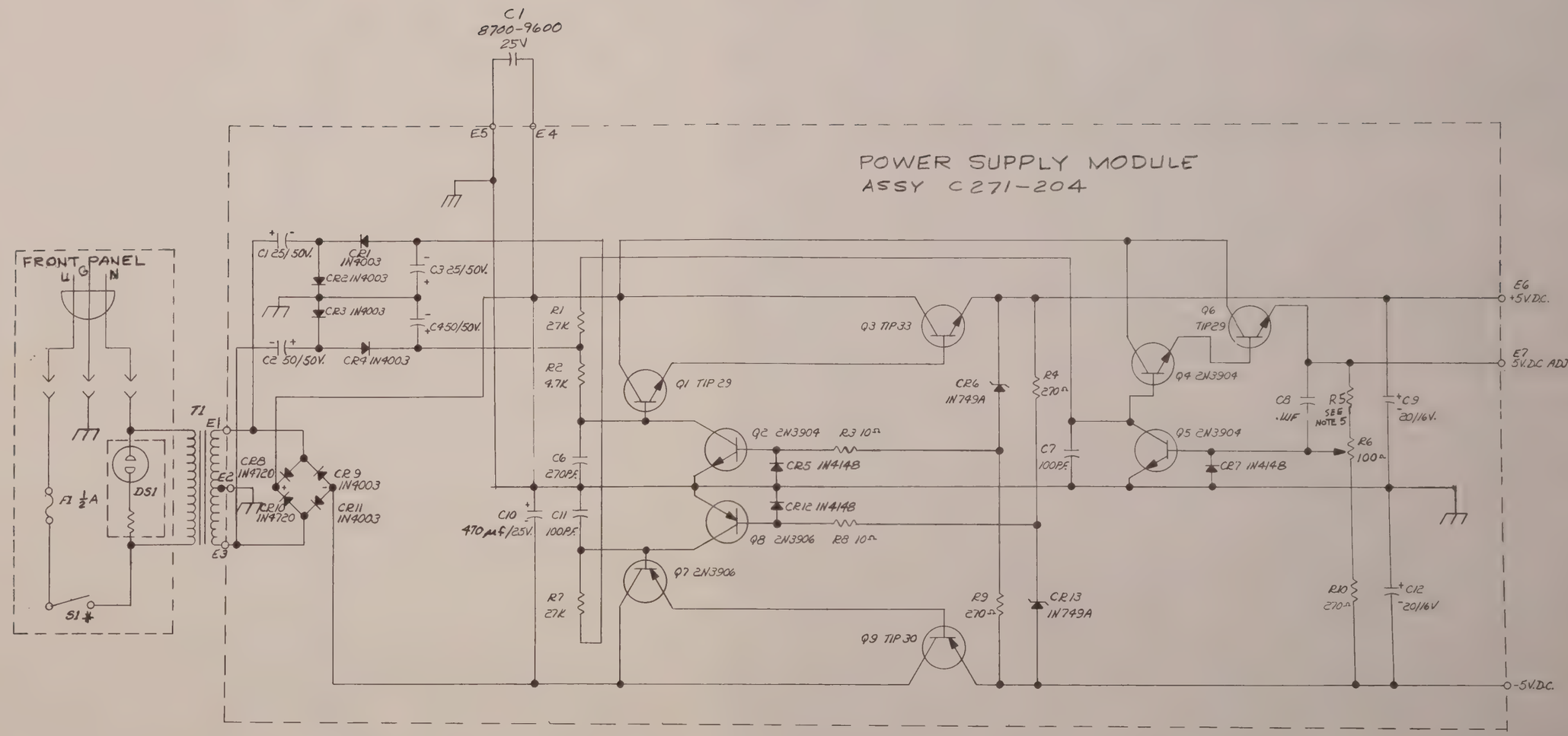
6.0 DRAWINGS

		Page
D271-104/K	Power Supply Schematic (A6)	6-2
C271-204/F	Power Supply Assembly (A6)	6-3
D271-120/B	Display Module Schematic (A8)	6-4
C271-220/N	Display Module Assembly (A8)	6-5
C271-221/L	Interconnect Assembly (A7)	6-6
D271-122/B	Receiver Reference Module Schematic (A1)	6-7
C271-222/D	Receiver Reference Module Assembly (A1)	6-8
D271-123/F	Receiver Logic Module Schematic (A2)	6-9
C271-223/F	Receiver Logic Module Assembly (A2)	6-10
D271-124/C	Auxiliary Module Schematic (A3)	6-11
C271-224/D	Auxiliary Module Assembly (A3)	6-12
D271-125/H	Receiver Module Schematic (A4)	6-13
C271-225/J	Receiver Module Assembly (A4)	6-14
D271-126/D	Transmitter Module Schematic (A5)	6-15
D271-226/E	Transmitter Module Assembly (A5)	6-16
D271-128/E	Main Schematic	6-17
E271-207/J	Main Assembly	6-18

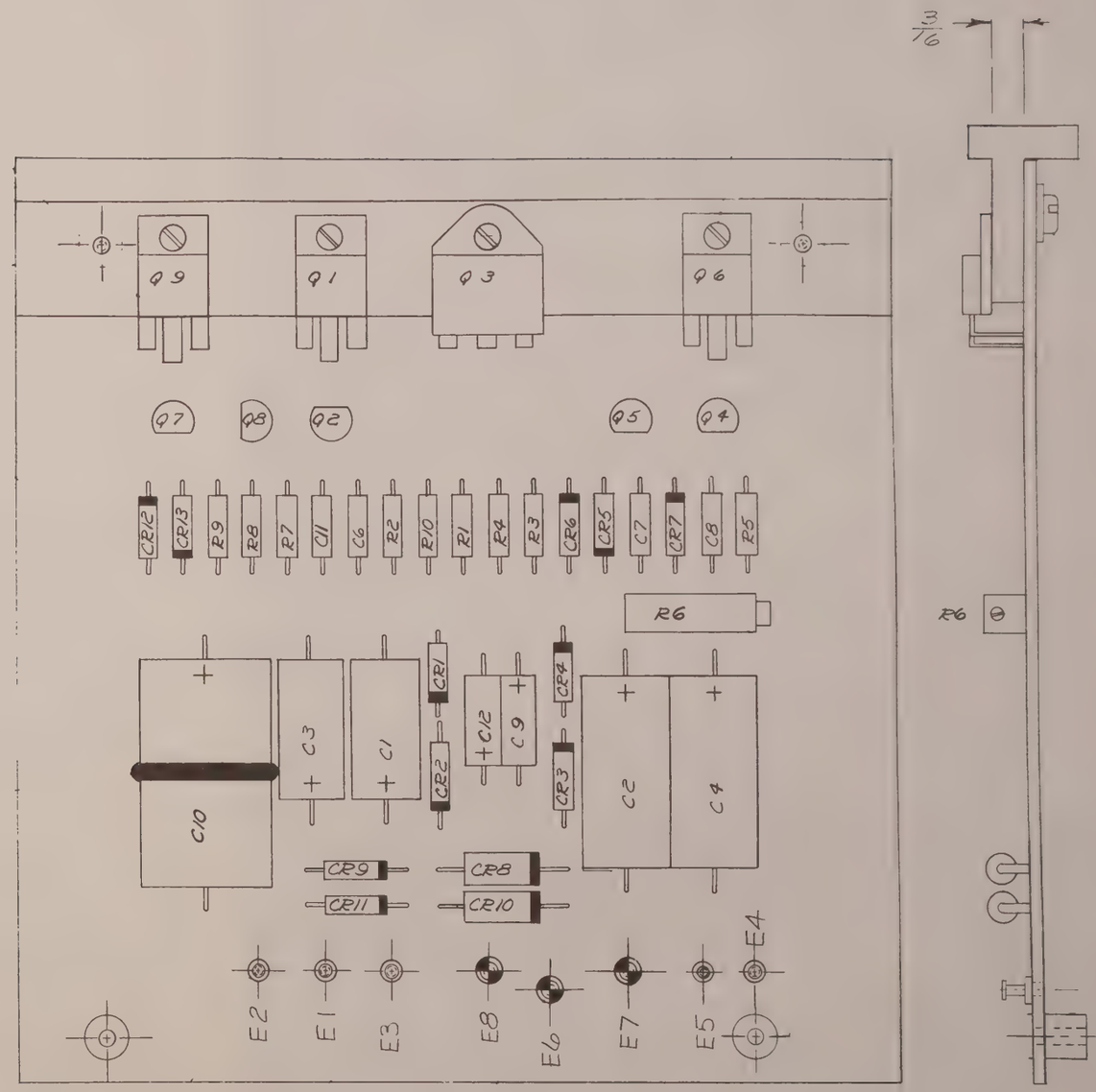
The drawings listed below are used in Serial Numbers below 600 and are included for reference only.

D271-123	Receiver Logic Module Schematic (A2)	6-20
C271-223	Receiver Logic Module Assembly (A2)	6-21
D271-125	Receiver Module Schematic (A4)	6-22
C271-225	Receiver Module Assembly (A4)	6-24

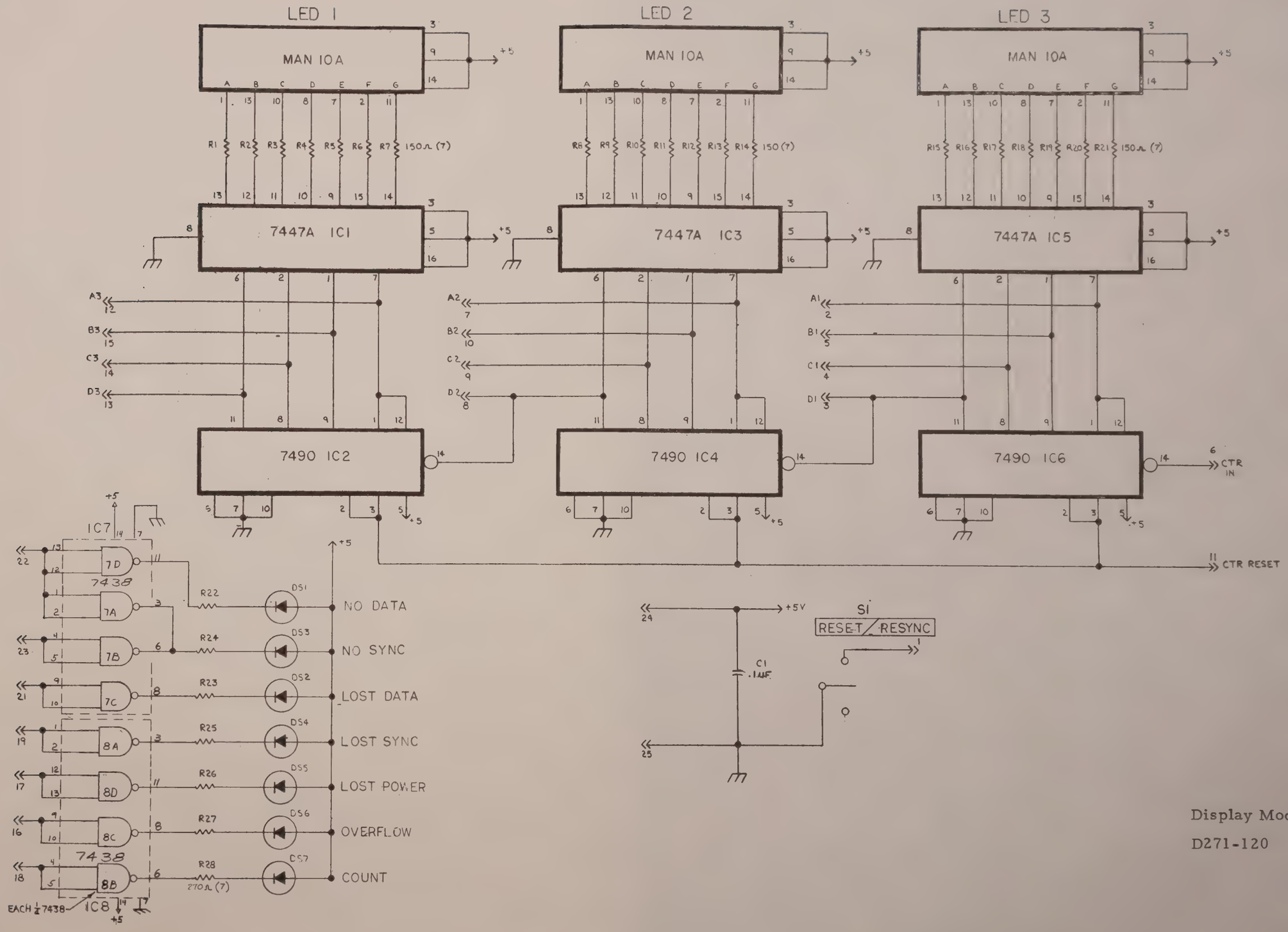
E4
E5
E7
E6
E8
E3
E1
E2
CR10
CR8
CR11
CR9
C4
C2
C12
C9
C1
C3
C10
CR3
CR4
CR2
CR1
R6
R5
C8
CR7
C7
CR5
CR6
R3
R4
R1
R10
R2
C6
C11
R7
R8
R9
CR13
CR12
Q4
Q5
Q2
Q8
Q7
Q6
Q3
Q1
Q9



Power Supply Schematic (A6)
D271-104

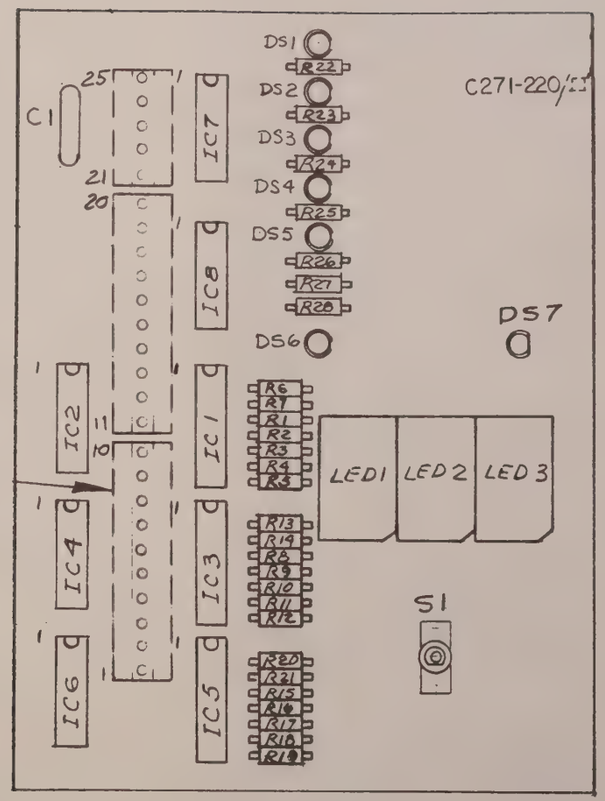


Power Supply Assembly (A6)
C271-204

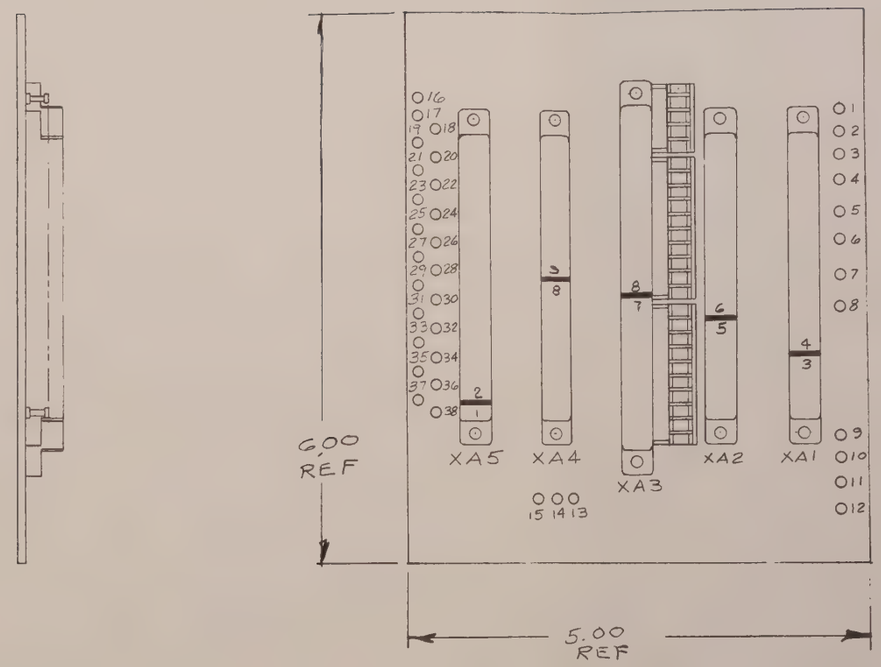


Display Module Schematic (A8)

D271-120

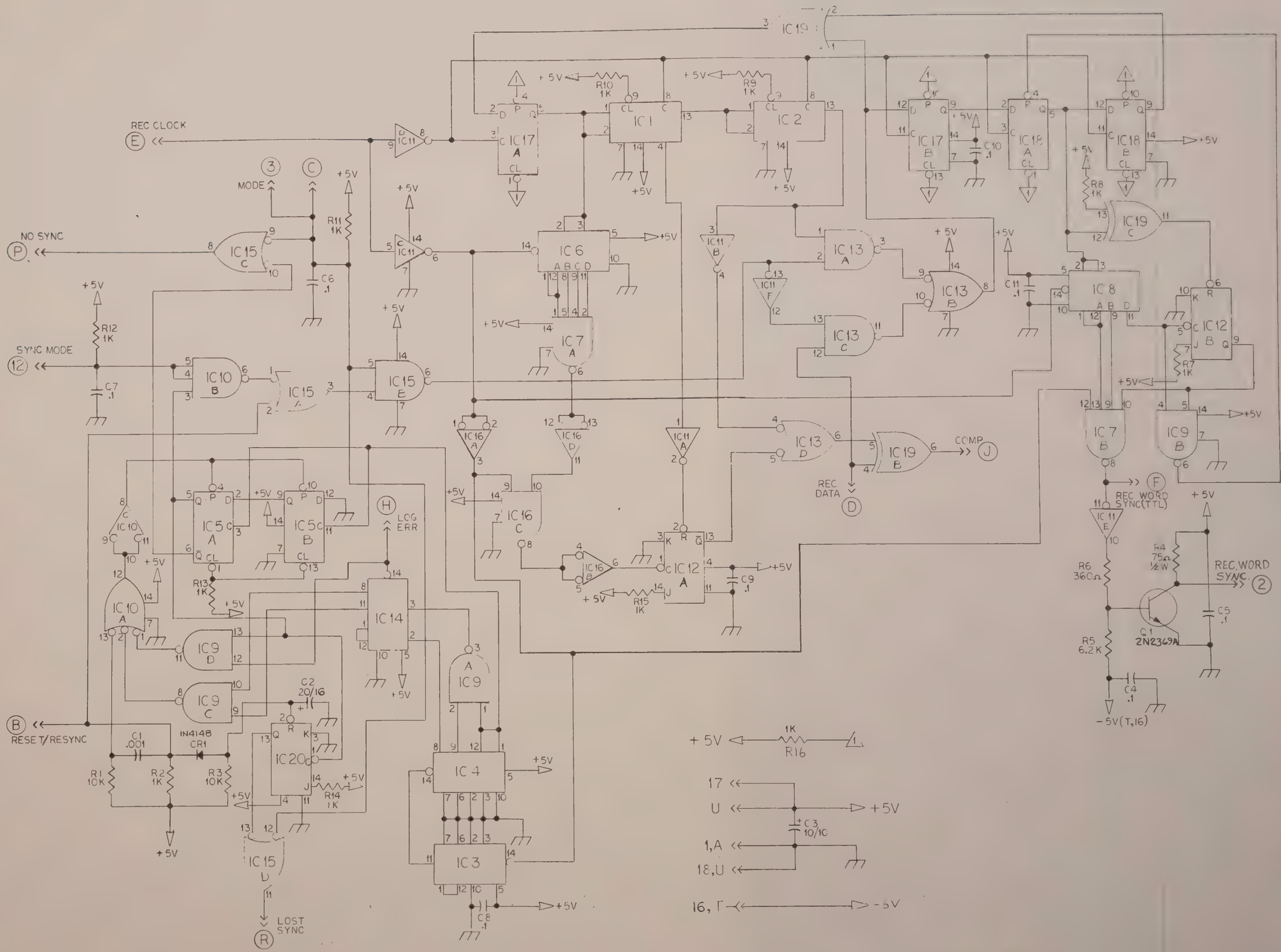


Display Module Assembly (A8)
C271-220



Interconnect Assembly (A7)

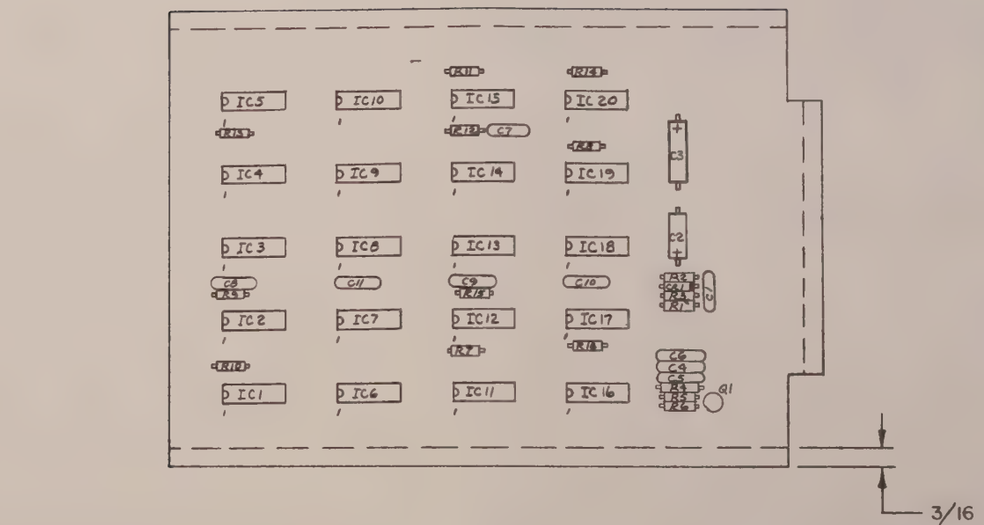
C271-221



I.C.		I.C.	
1	74164	11	7404
2	74164	12	7473
3	7490	13	7400
4	7490	14	7493
5	7474	15	7400
6	7493	16	7400
7	7420	17	7474
8	7493	18	7474
9	7400	19	7486
10	7410	20	7473

Receiver Reference Module Schematic (A1)

D271-122



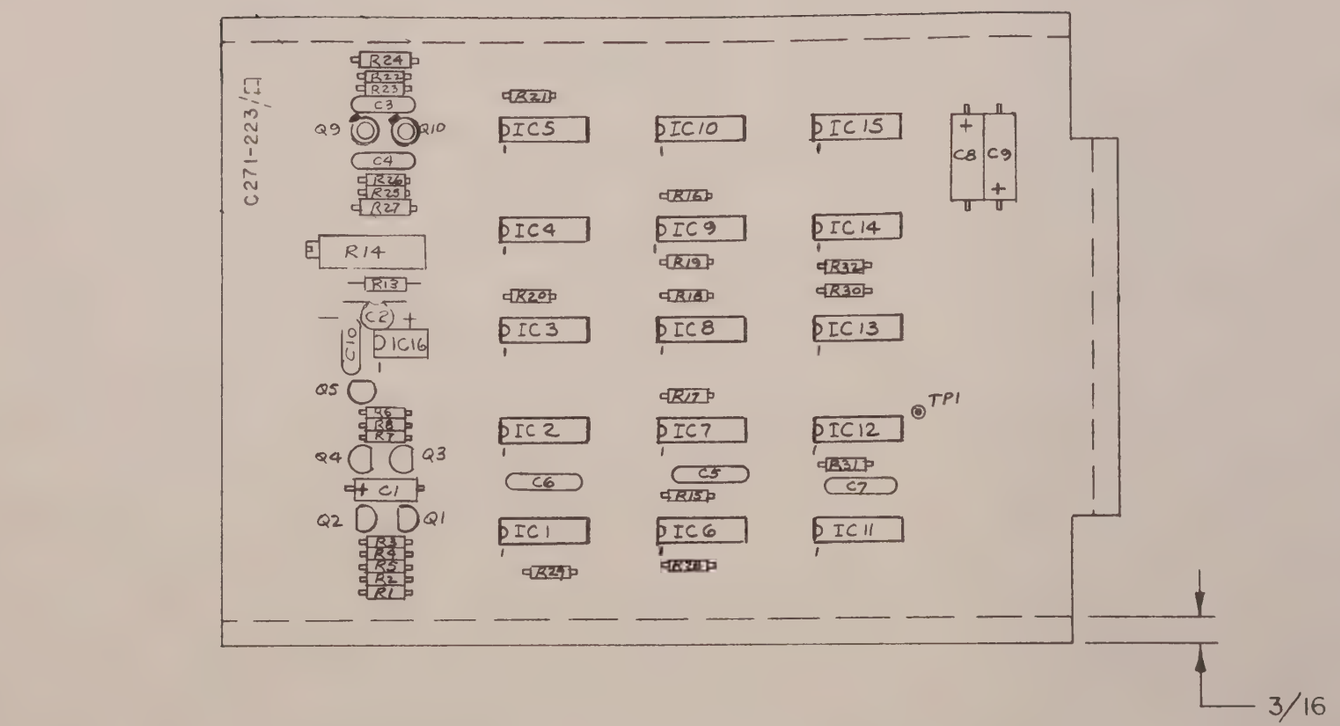
Receiver Reference
Module Assembly (A1)

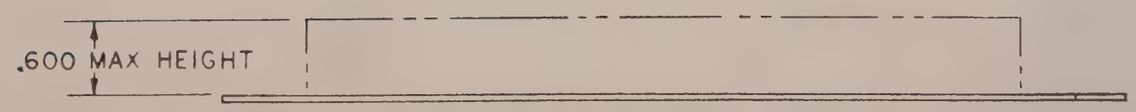
C271-222

IC	
1	7490
2	7490
3	7400
4	7410
5	7473
6	7400
7	7473
8	7404
9	7400
10	7400
11	7474
12	7473
13	7474
14	7404
15	7400
16	LM555

Receiver Logic Module Schematic (A2)

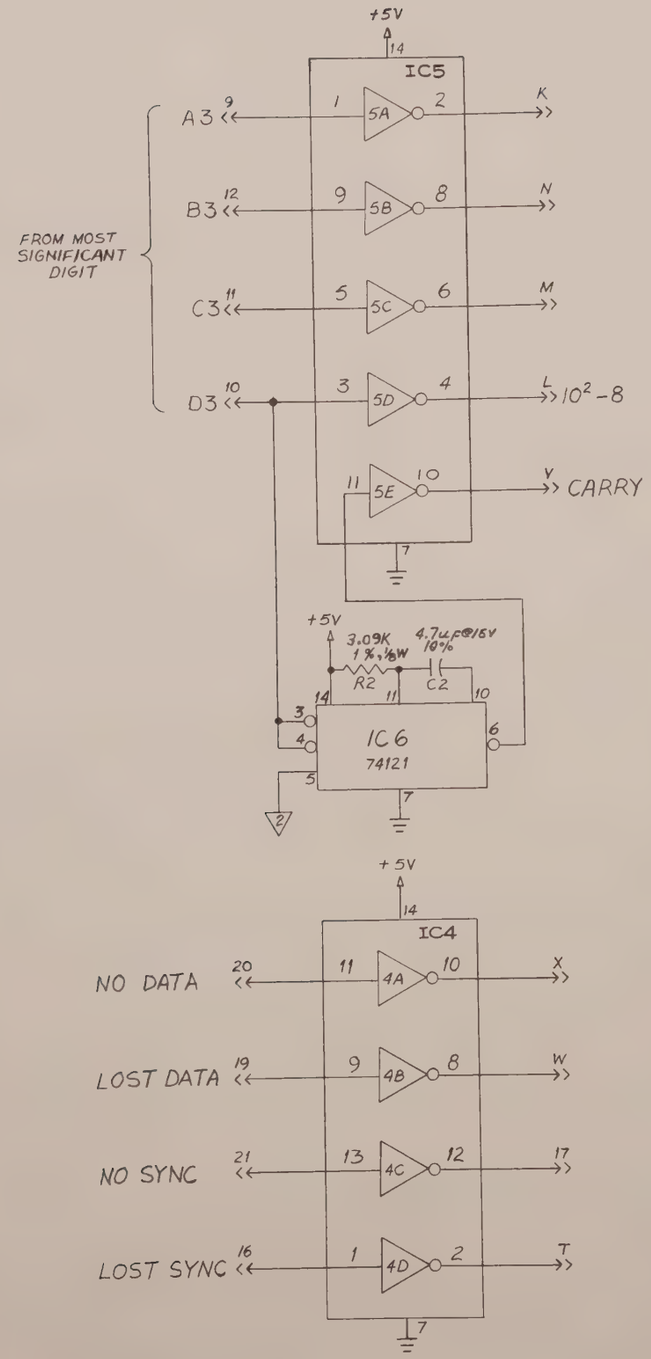
D271-123

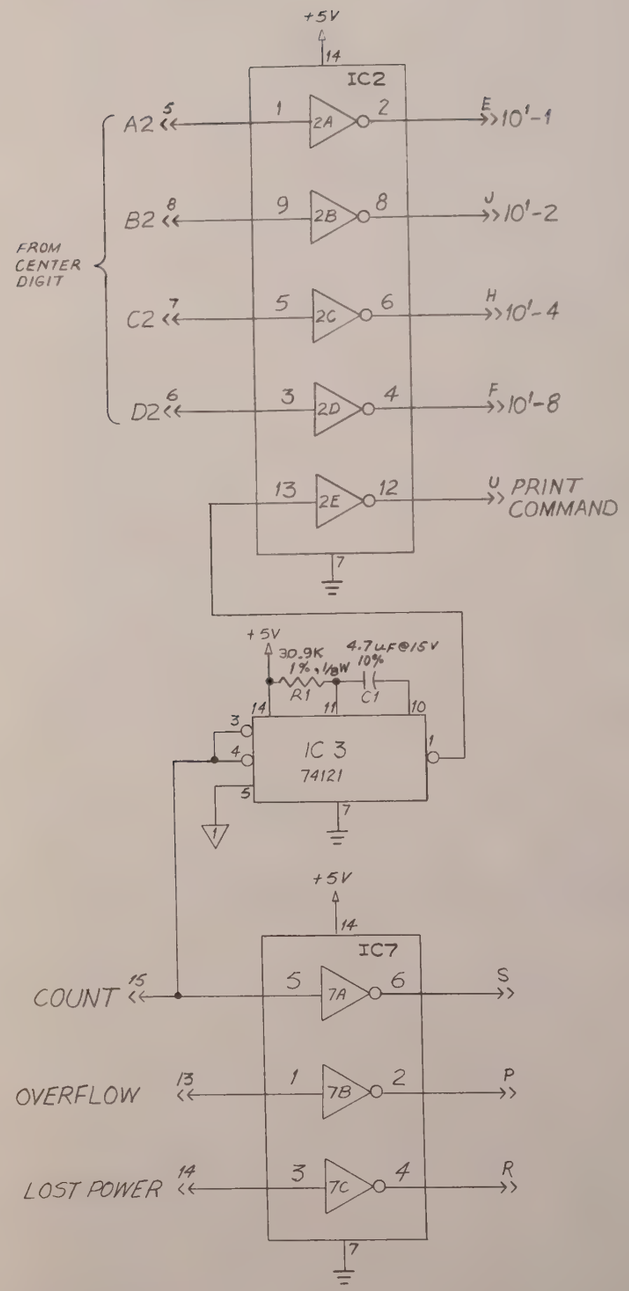


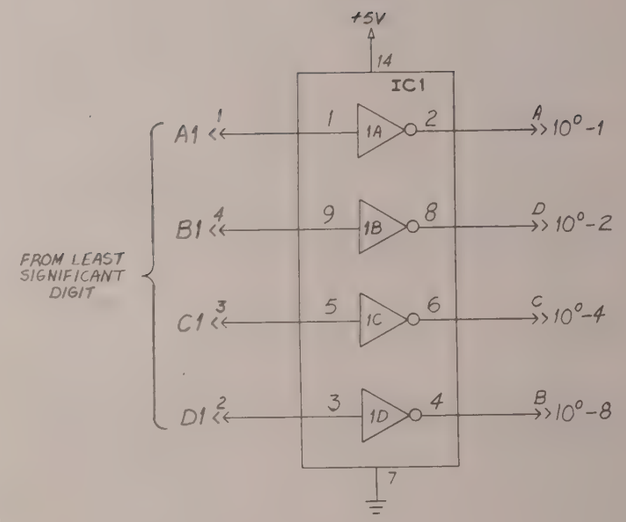


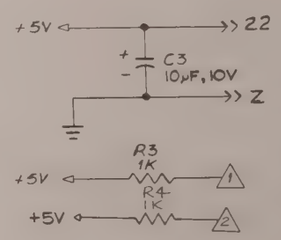
Receiver Logic
Module Assembly (A2)

C271-223



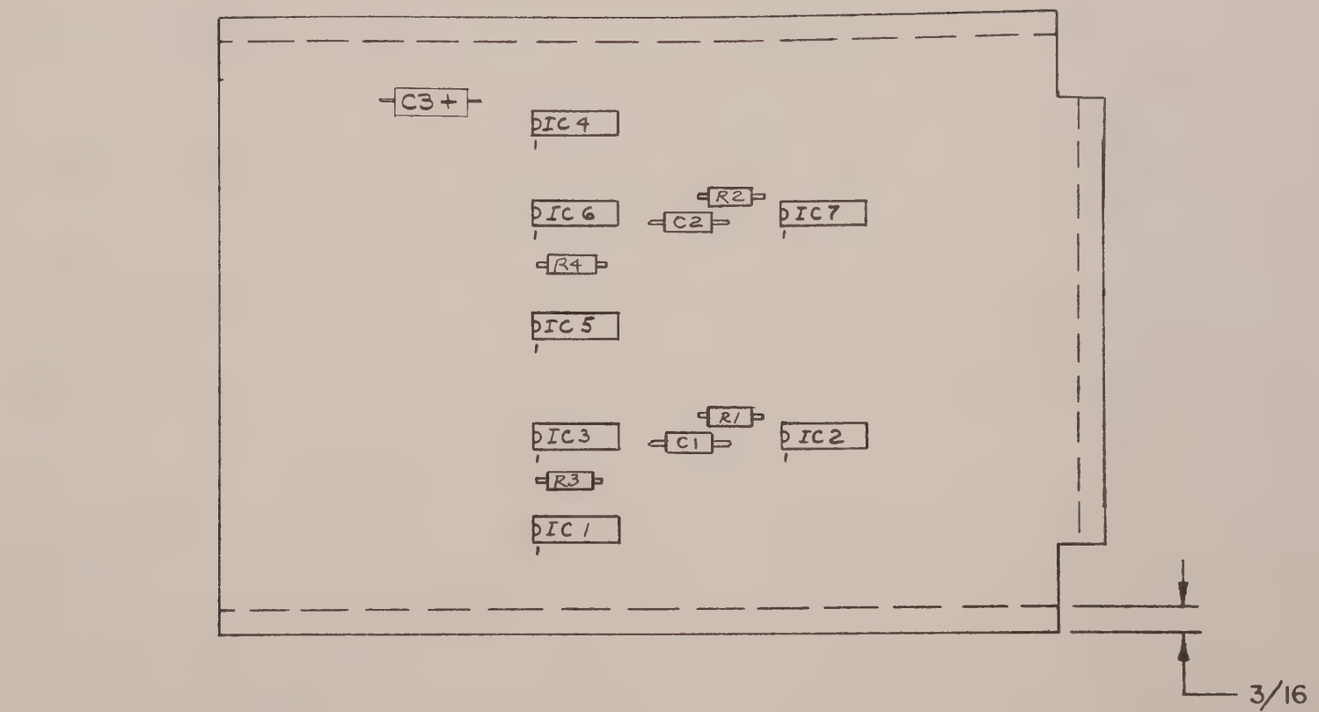




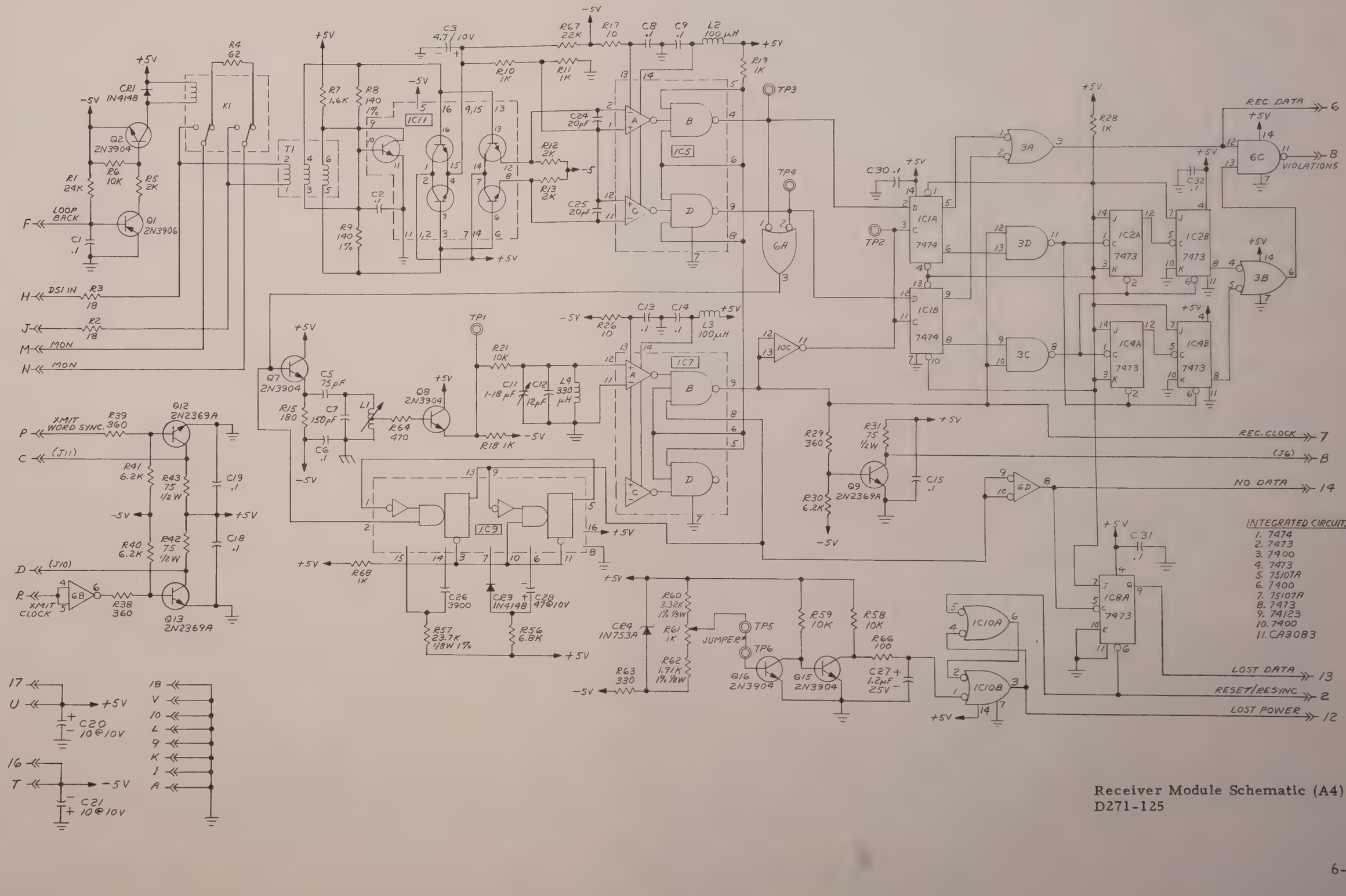


Auxiliary Module Schematic (A3)

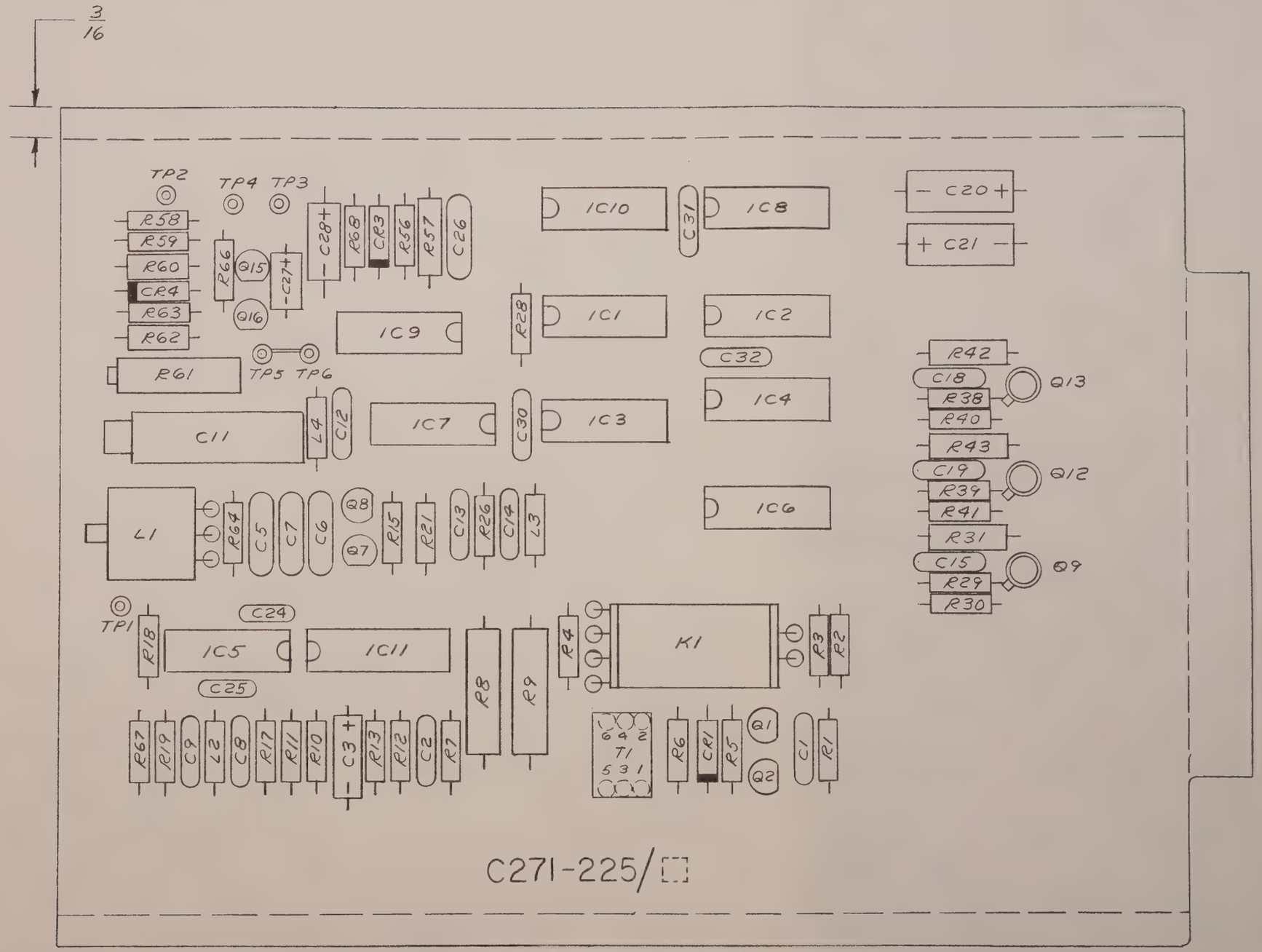
D271-124



Auxiliary Module Assembly (A3)
C271-224



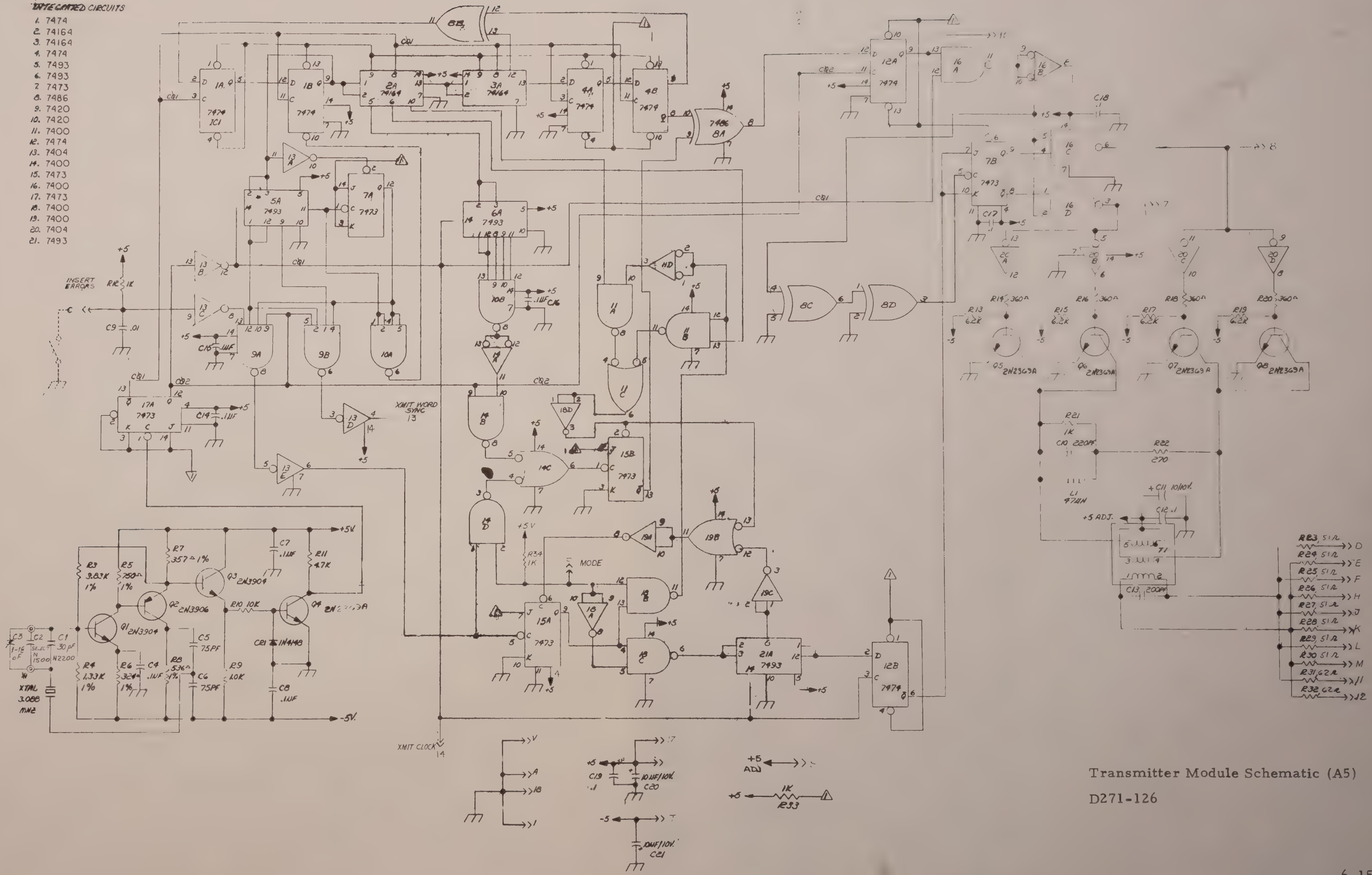
Receiver Module Schematic (A4)
D271-125



Receiver Module Assembly (A4)
C271-225

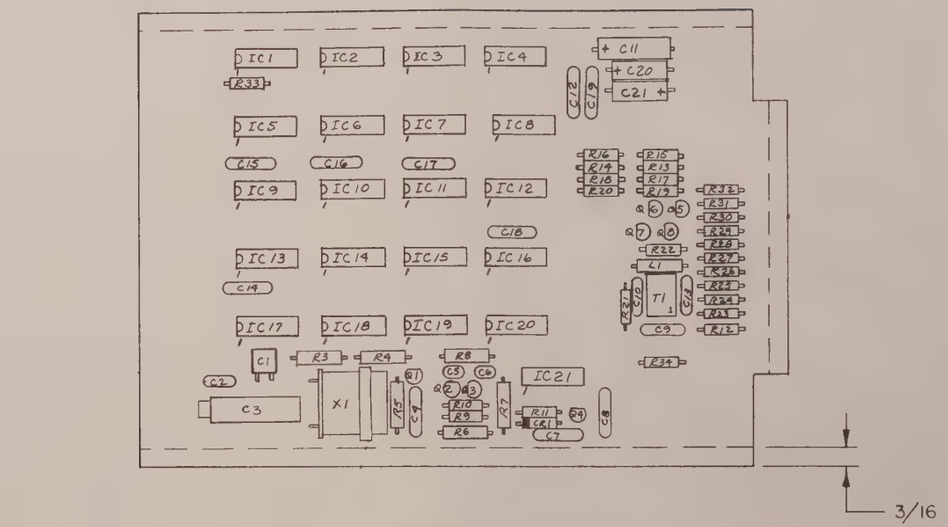
INTEGRATED CIRCUITS

1. 7474
2. 74164
3. 74164
4. 7474
5. 7493
6. 7493
7. 7473
8. 7486
9. 7420
10. 7420
11. 7400
12. 7474
13. 7404
14. 7400
15. 7473
16. 7400
17. 7473
18. 7400
19. 7400
20. 7404
21. 7493



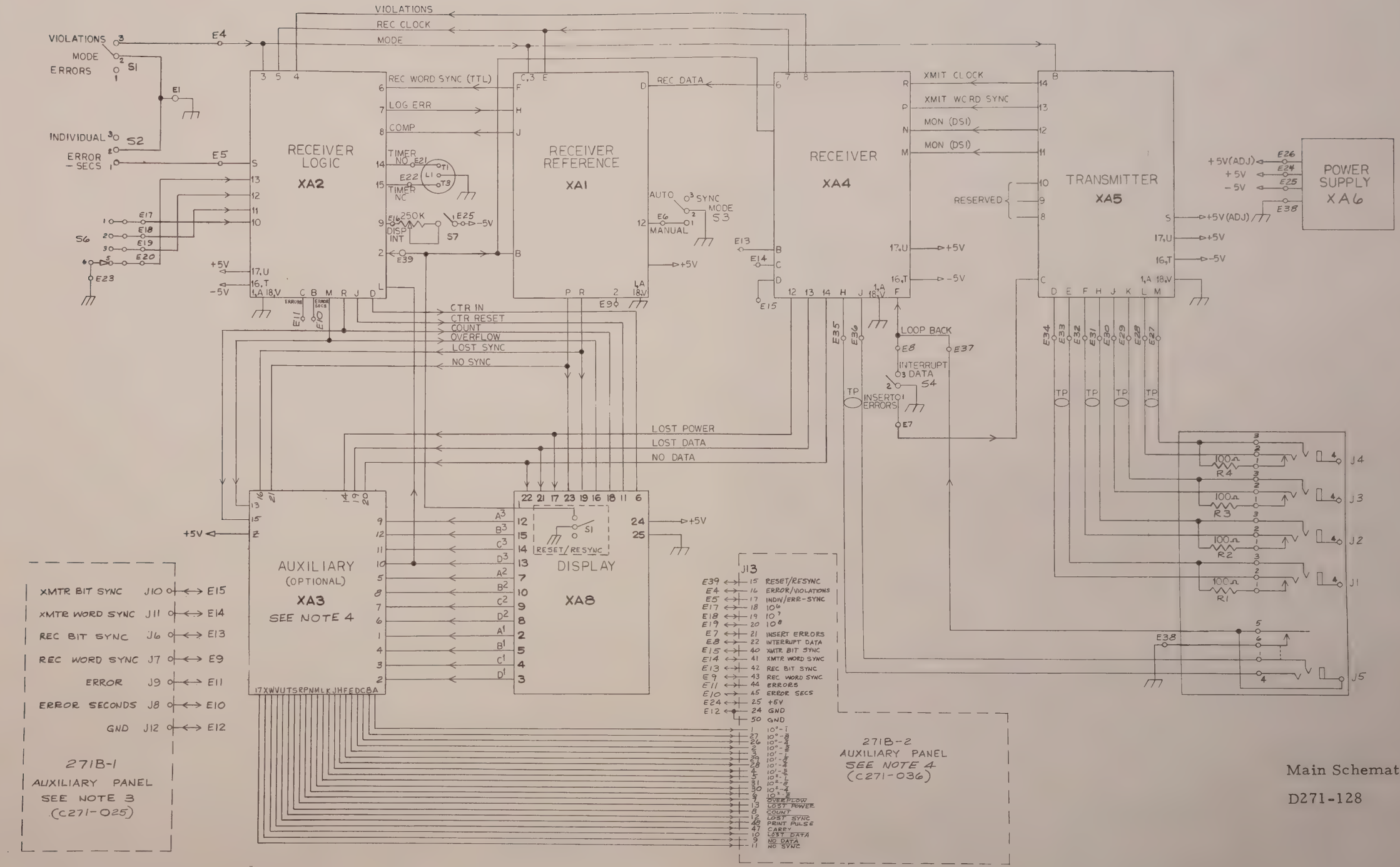
Transmitter Module Schematic (A5)

D271-126



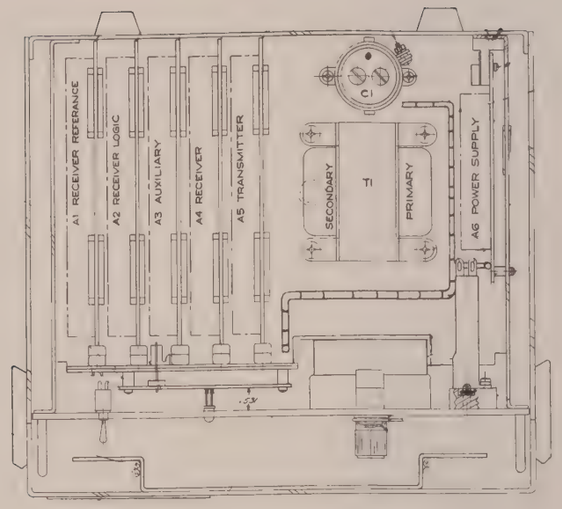
Transmitter Module Assembly (A5)

D271-226

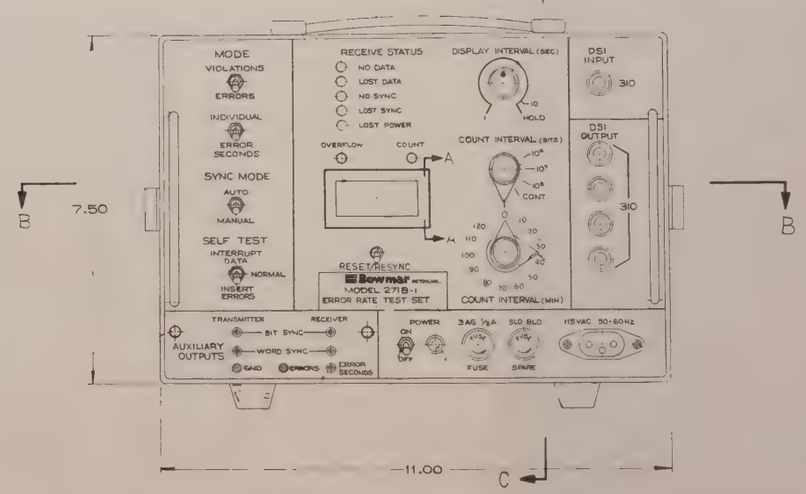


Main Schematic

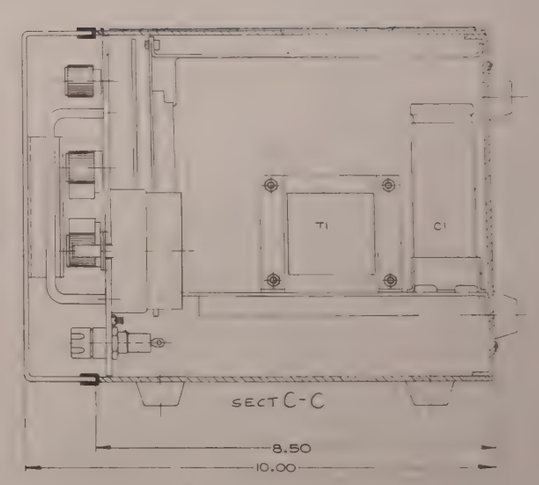
D271-128



SECT B-B



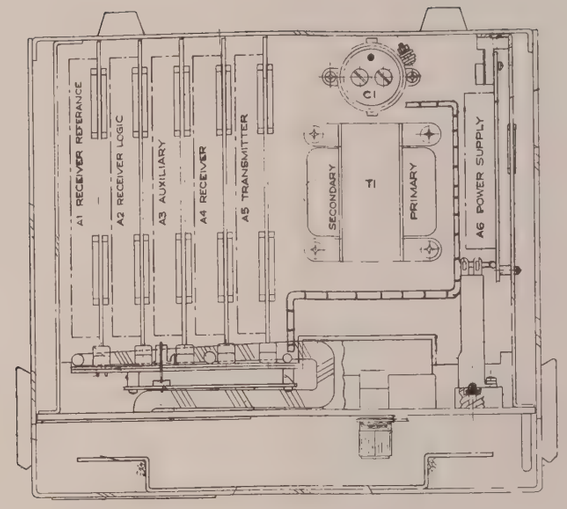
SHOWN WITH COVER REMOVED



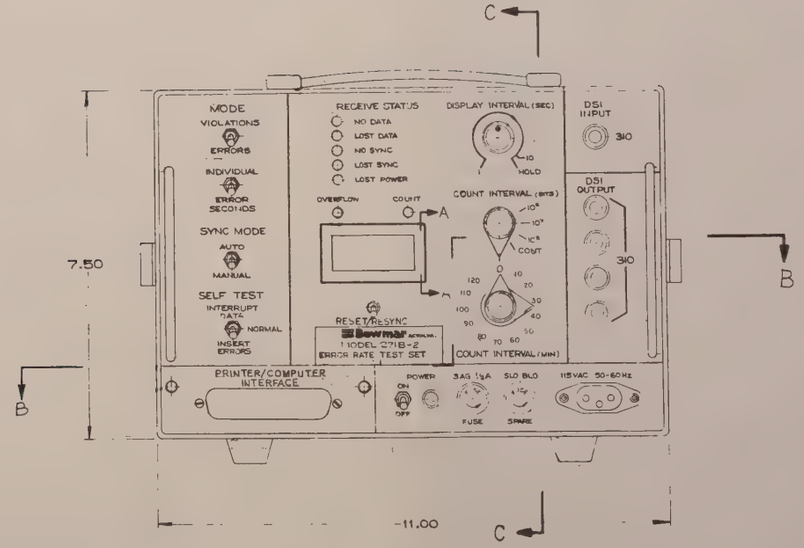
SHEET 1 OF 2 FOR 271B-1

SEE SHEET 2 OF 2 FOR 271B-2

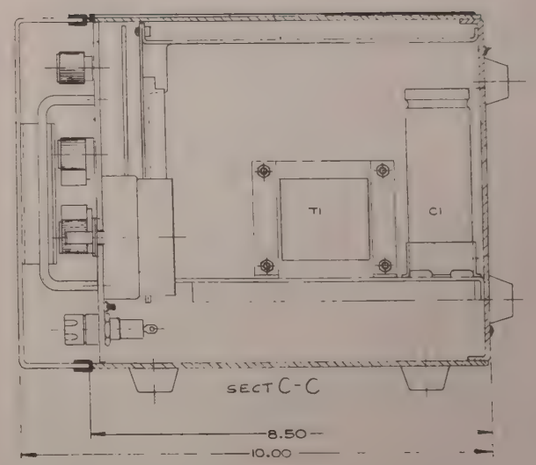
Main Assembly
E271-207 (Sheet 1 of 2)



SECT B-B



SHOWN WITH COVER REMOVED



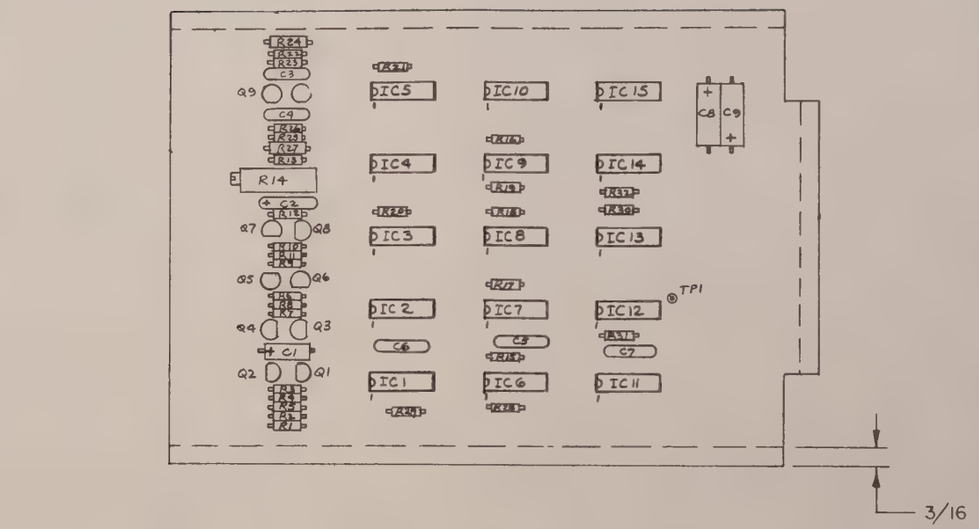
SHEET 2 271B-2

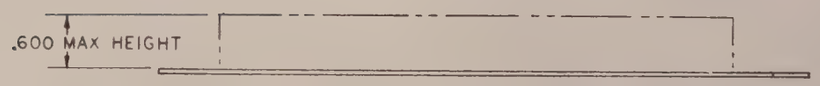
Main Assembly
E271-207 (Sheet 2 of 2)

1 C	
1	7490
2	7490
3	7400
4	7410
5	7473
6	7400
7	7473
8	7404
9	7400
10	7400
11	7474
12	7473
13	7474
14	7404
15	7400

Receiver Logic
Module Schematic (A2)

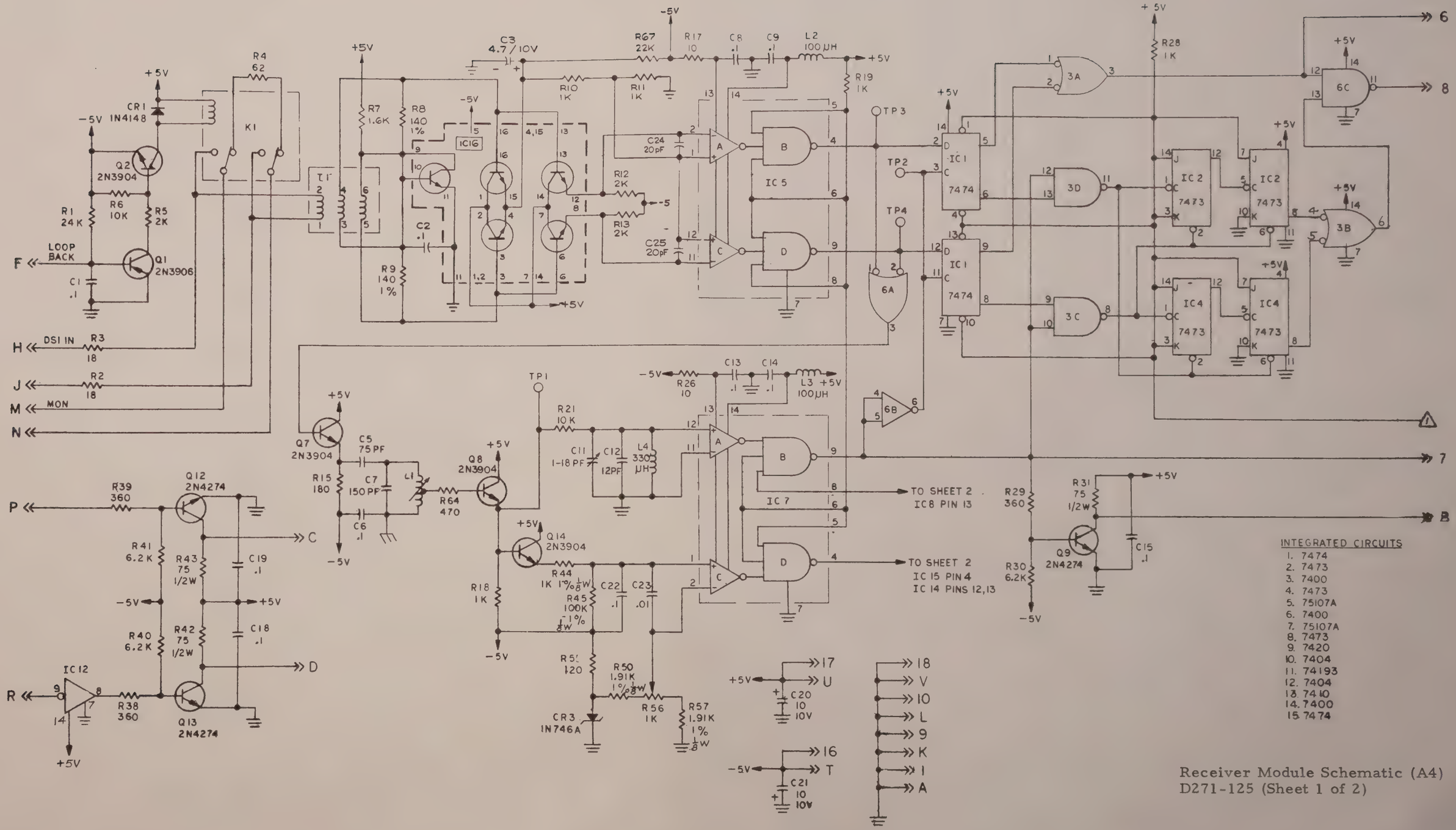
D271-123



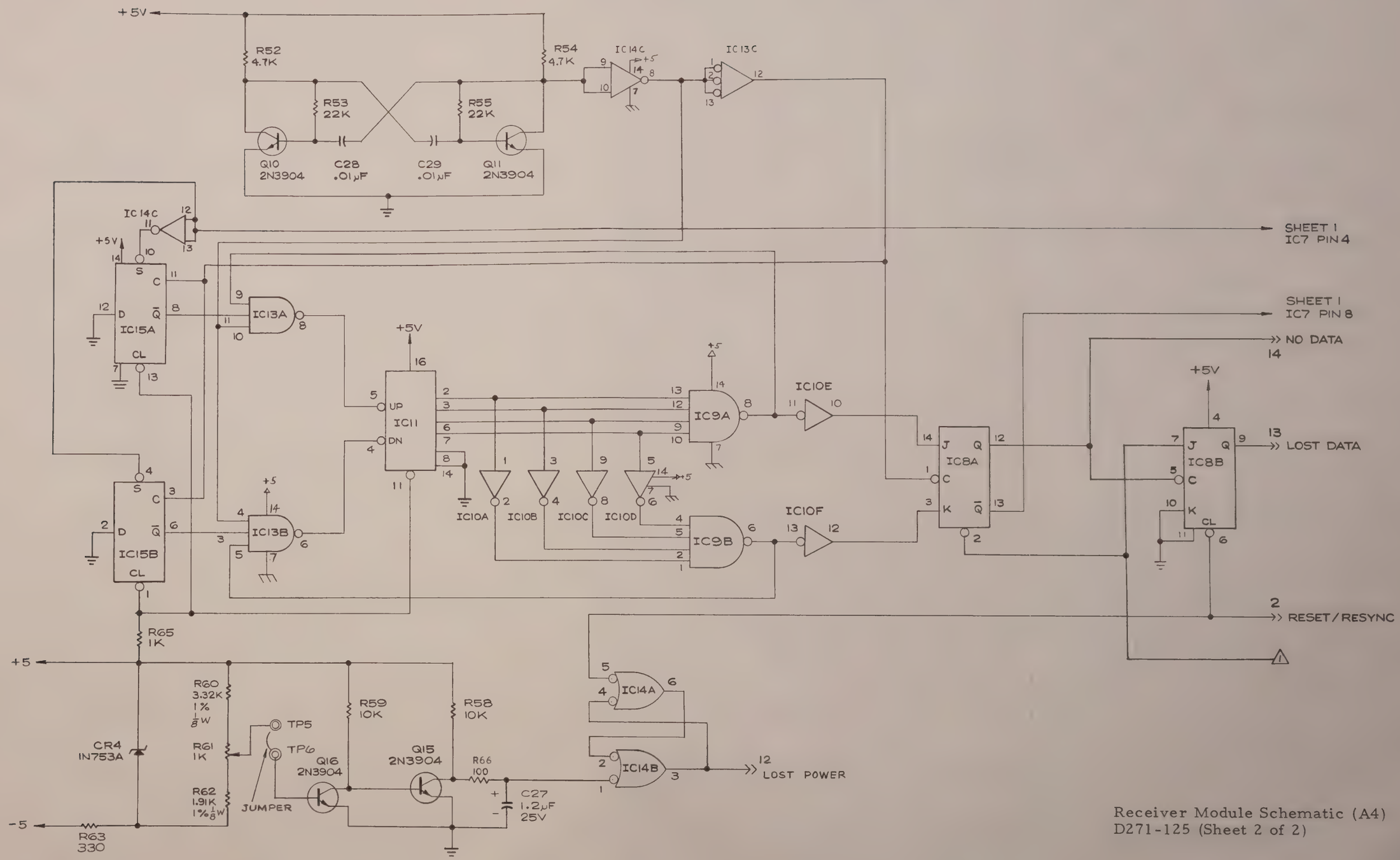


Receiver Logic
Module Assembly (A2)

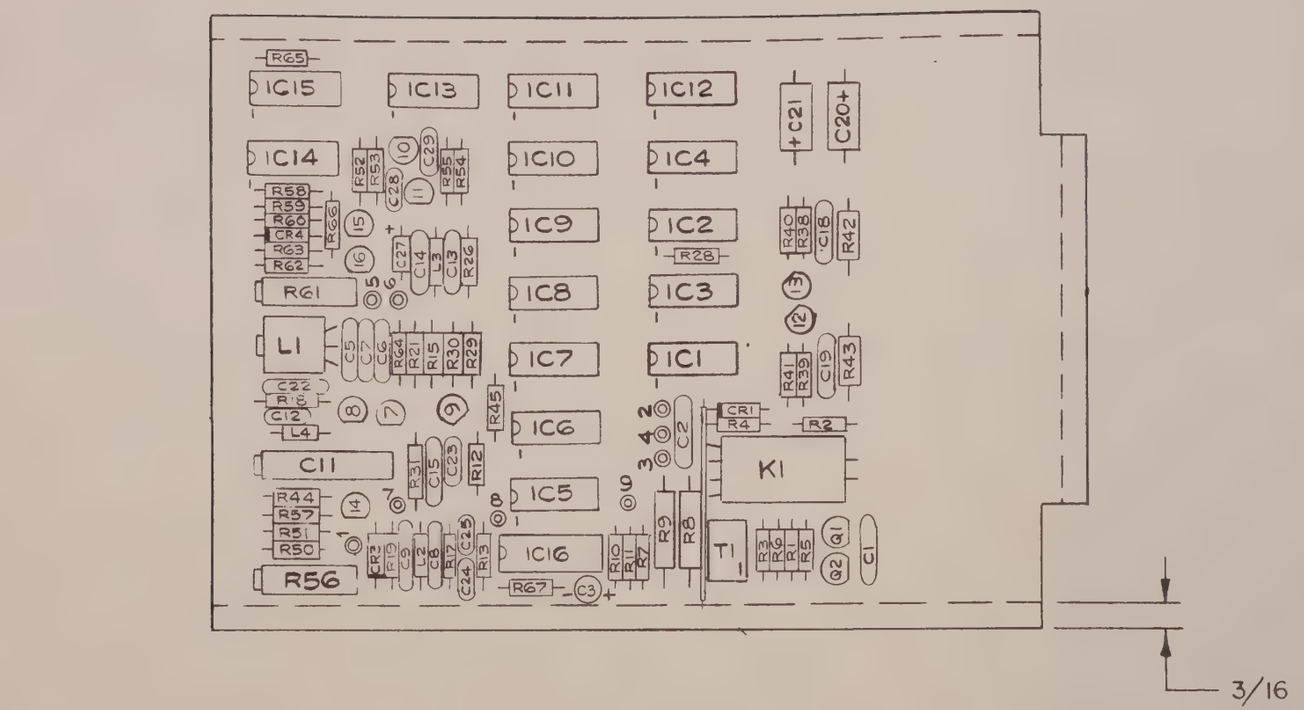
C271-223



Receiver Module Schematic (A4)
D271-125 (Sheet 1 of 2)



Receiver Module Schematic (A4)
D271-125 (Sheet 2 of 2)



Receiver Module Assembly (A4)

C271-225

7.0 PARTS LIST

7.1 General

The Parts List identifies and describes all electrical parts for the Error Rate Test Set. The manufacturer's name and part number is included except where the item is a standardized RETMA part, in which case the product of a registered manufacturer should be acceptable. Items with ALI part numbers are purchased to the Bowmar/ALI Specification Control Drawing. The List of Manufacturers includes abbreviations used in the Parts List, as well as complete addresses.

REF. DESIGNATION	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NUMBER
POWER SUPPLY BOARD ASSEMBLY (A6) (271-204)			
CR1,2,3,4,9,11	Diode Rectifier, 1 Amp		1N4003
CR8, 10	Diode Rectifier, 3 Amp		1N4720
CR5, 7, 12	Diode		1N4148
CR6, 13	Diode, Zener		1N749A
Q1, 6	Transistor, With Mica Insulator & Shoulder Washer	T.I.	TIP-29
Q9	Transistor, With Mica Insulator & Shoulder Washer	T.I.	TIP-30
Q3	Transistor, With Mica Insulator & Shoulder Washer	T.I.	TIP-33
Q2, 4, 5	Transistor NPN		2N3904
Q7, 8	Transistor PNP		2N3906
R2	Resistor, 4.7K, 1/2W, 5%		RCR20G472JS
R4, 9, 10	Resistor, 270, 1/2W, 5%		RCR20G271JS
R3, 8	Resistor, 10, 1/2W, 5%		RCR20G100JS
R1, 7	Resistor, 27K, 1/2W, 5%		RCR20G273JS
R5	Resistor, 300, 1/2W, 5%		RCR20G301JS
R6	Potentiometer, 100 Ohm	Beckman or Bourns	89PR100 or 3006P-1-101
C2, 4	Capacitor, 47 uf, 50V or 50 uf, 50V	Capar or Sprague	CAE-E47M50V or TE-1307E
C1, 3	Capacitor, 25 uf, 50V	CDE	NLW25-50E
C9, 12	Capacitor, 20 uf, 16V	CDE	NLW20-16E
C8	Capacitor, .1 uf, 16V	Centralab	UK-16-104
C10	Capacitor, 470 uf, 25V	Capar or Siemens	CAE-E470M25V or 470/25/82006
C7, 11	Capacitor, 100 pf	CDE	CD10FD101J03
C6	Capacitor, 270 pf	CDE	CD10FC271J03

REF. DESIGNATION	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NUMBER
MAIN ASSEMBLY (271-032, 271-208, 271-250, 271-251)			
R1 - R4	Resistor, 100, 1/4W, 5%		RCR07G101JS
J1,2,3,4	Phone Jack	Switchcraft	MT-333B
J5	Phone Jack	Switchcraft	MT-336B
S1,2,3,5	Switch, SPDT	C & K	7101SPHZQE
S4	Switch, Momentary	C & K	7105SPHZQE
S6	Switch, Subminiature, Rotary, 0 Index, 5 Position	Bowmar/ALI	B6439-1
S7-R1	Variable Resistor & AC Switch	Bowmar/ALI	B6220-1
DS1	Lamp, Glo-Dot	Industrial Devices	2150A1
XF1, XF2	3 A G Fuse Extractor Post	Littlefuse	342014A
F1, F2	3 A G S10-Blo Fuse 1/2 Amp	Littlefuse	313500
P1	Receptacle	Switchcraft	EAC-302
M1	Timer	Bowmar/ALI	C6393-1
C1	Capacitor, Electrolytic, 8700uf, 25 VDC	G.E. or Sprague	86F139M or 36D8226025AC2A
T1	Transformer	Bowmar/ALI	B6218
GRD (J12)	Terminal, GND	Bowmar/ALI	B4850
J6 - J11	Insulated Jack	Sealectro	SKT-5BC Gray

REF. DESIGNATION	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NUMBER
DISPLAY P.C. BOARD (A8) (271-220)			
IC1, 3, 5	Integrated Circuit TTL		SN7447AN
IC2, 4, 6	Integrated Circuit TTL		SN7590AN
IC7, 8	Integrated Circuit TTL		SN7438N
LED 1, 2, 3	LED, 7 Segment	G.I.	MAN-72A
R1 - R21	Resistor, 150, 1/4W, 5%		RCR07G151JS
C1	Capacitor, 0.1 uf, 16V, Disc.	Centralab	UK-16-104
DS1 - DS7	LED	Hewlett Packard	HLMP 3300
S1	Switch, Toggle Momentary	C & K	7109SPV30CQE
R22-28	Resistor, 270, 1/4W, 5%		RC07GF271J
INTERCONNECTION BOARD ASSEMBLY (A7) (271-221)			
XA1, 2, 4, 5	Double Readout Connector Printed Circuit Mtg. 18 Pins	Cinch	252-18-30-160
XA3	Double Readout Connector Printed Circuit Mtg. 22 Pins	Cinch	252-22-30-160
E1 - E39	Solder Terminal	Cambion	160-2027-02-01-00
RECEIVER REFERENCE P.C. BOARD (A1) (271-222)			
IC9, 13, 15, 16	Integrated Circuit TTL		SN7400N
IC11	Integrated Circuit TTL		SN7404N
IC10	Integrated Circuit TTL		SN7410N
IC7	Integrated Circuit TTL		SN7420N
IC12, 20	Integrated Circuit TTL		SN7473N
IC5, 17, 18	Integrated Circuit TTL		SN7474N
IC19	Integrated Circuit TTL		SN7486N
IC3, 4	Integrated Circuit TTL		SN7490AN
IC6, 8, 14	Integrated Circuit TTL		SN7493AN
IC1, 2	Integrated Circuit TTL		SN74164N
Q1	Transistor		2N2369A
CR1	Diode		1N4148

REF. DESIGNATION	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NUMBER
RECEIVER REFERENCE P.C. BOARD (A1) (271-222) (Con't)			
R1, 3	Resistor, 10K, 1/4W, 5%		RCR07G103JS
R2,7,8,9,10,11,12, R13, 14, 15, 16	Resistor, 1K, 1/4W, 5%		RCR07G102JS
R5	Resistor, 6.2K, 1/4W, 5%		RCR07G622JS
R4	Resistor, 75, 1/2W, 5%		RCR20G750JS
R6	Resistor, 360, 1/4W, 5%		RCR07G361JS
C1	Capacitor, .001 uf Disc.	Centralab	DD-102
C3	Capacitor, 10 uf, 16V	CDE	NLW-10-16E
C4,5,6,7,8,9,10,11	Capacitor, 0.1 uf, 16V, Disc.	Centralab	UK-16-104
C2	Capacitor, 20 uf, 16V	CDE	NLW-20-16
RECEIVER LOGIC P.C. BOARD (A2) (271-223)			
IC3, 6, 9, 10, 15	Integrated Circuit TTl		SN7400N
IC8, 14	Integrated Cirucit TTL		SN7404N
IC4	Integrated Circuit TTL		SN7410N
IC5, 7, 12	Integrated Circuit TTL		SN7473N
IC11, 13	Integrated Circuit TTL		SN7474N
IC1, 2	Integrated Circuit TTL		SN7490AN
IC16	Integrated Circuit Timer	National or Signetics or Fairchild or Silicon General or RCA or Motorola	LM555CN or NE555V or SG555CM or CA555CE or MC1455P
R1, 3, 8	Resistor, 10K, 1/4W, 5%		RCR07G103JS
R2, 4	Resistor, 3.3K, 1/4W, 5%		RCR07G332JS
R5	Resistor, 24K, 1/4W, 5%		RCR07G243JS
R6	Resistor, 4.7K, 1/4W, 5%		RCR07G472JS
R13	Resistor, 220, 1/4W, 5%		RCR07G221JS
R14	Potentiometer, 100K	Bourns or Beckman	3006W-1-104 or 89WR100K

REF. DESIGNATION	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NUMBER
RECEIVER LOGIC P.C. BOARD (A2) (271-223) (Con't)			
R15-21, R30, 31, 32	Resistor, 1K, 1/4W, 5%		RCR07G102JS
R22, 25	Resistor, 6.2K, 1/4W, 5%		RCR07G622JS
R23, 26	Resistor, 360, 1/4W, 5%		RCR07G361JS
R24, 27	Resistor, 75, 1/2W, 5%		RCR20G750JS
R28, 29	Resistor, 470, 1/4W, 5%		RCR07G471JS
R7	Resistor, 2K, 1/4W, 5%		RCR07G202JS
C1	Capacitor, 40 uf, 10V or 39 uf, 10V	Sprague	150D406X9010B2 or 150D396X9010B2
C2	Capacitor, 10 uf, 10V	Sprague or Equiv.	196D106X9010JA1 or 196D106X9020JA1
C3, 4, 5, 6, 7	Capacitor, 0.1 uf, 16V Disc.	Centralab	UK-16-104
C8, 9	Capacitor, 10 uf, 16V	CDE	NLW10-16E
C10	Capacitor, .01 uf ± 10%	Unitrode	CGC103KDX
Q3, 5	Transistor		2N3904
Q1, 2, 4	Transistor		2N3906
Q9, 10	Transistor		2N2369A
TP1	Terminal, Turret	Cambion	160-2027-02-01-00
RECEIVER P.C. BOARD (A4) (271-225)			
IC3, 6, 10	Integrated Circuit TTL		SN7400N
IC2, 4, 8	Integrated Circuit TTL		SN7473N
IC1	Integrated Circuit TTL		SN7474N
IC5, 7	Integrated Circuit Line Receiver		SN75107AN
IC9	Integrated Circuit TTL		SN74123N
IC11	Transistor Array NPN	RCA	CA3083
Q1	Transistor (Not MPS)		2N3906
Q2,7,8,15,16	Transistor (Not MPS)		2N3904
Q9, 12, 13	Transistor NPN		2N2369A

REF. DESIGNATION	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NUMBER
RECEIVER P.C. BOARD (A4) (271-225) (Con't)			
CR1, 3	Diode		1N4148
CR4	Diode, Zener, 6.2V, 5%		1N753A
R1	Resistor 24K, 1/4W, 5%		RCR07G243JS
R2, 3	Resistor, 18, 1/4W, 5%		RCR07G180JS
R4	Resistor, 62, 1/4W, 5%		RCR07G620JS
R5, 12, 13	Resistor, 2K, 1/4W, 5%		RCR07G202JS
R6, 21, 58, 59	Resistor, 10K, 1/4W, 5%		RCR07G103JS
R10,11,18,19,28,68	Resistor, 1K, 1/4W, 5%		RCR07G102JS
R8, 9	Resistor, 140, 1/4W, 1%		RN65C1400F
R15	Resistor, 180, 1/4W, 5%		RCR07G181JS
R17, 26	Resistor, 10, 1/4W, 5%		RCR07G100JS
R29, 38, 39	Resistor, 360, 1/4W, 5%		RCR07G361JS
R31, 42, 43	Resistor, 75, 1/2W, 5%		RCR20G750JS
R40, 41, 30	Resistor, 6.2K, 1/4W, 5%		RCR07G622JS
R66	Resistor, 100, 1/4W, 5%		RCR07G101JS
R60	Resistor, 3.32K, 1/8W, 1%		RN60C3321F
R62	Resistor, 1.91K, 1/8W, 1%		RN60C1911F
R63	Resistor, 330, 1/4W, 5%		RCR07G331JS
R64	Resistor, 470, 1/4W, 5%		RCR07G471JS
R67	Resistor, 22K, 1/4W, 5%		RCR07G223JS
R7	Resistor, 1.6K, 1/4W, 5%		RCR07G162JS
R56	Resistor, 6.8K, 1/4W, 5%		RCR07G682JS
R57	Resistor, 23.7K, 1/8W, 1%		RN60C2372F
R61	Potentiometer, 1K, 3/4W	Bourns or Beckman	3006W-1-102 or 89WR1K
C1,6,8,9,13,2,14,15, C18,19,30,31,32	Capacitor, 0.1 uf, 16V Disc.	Centralab	UK-16-104
C20, 21	Capacitor, 10 uf, 16V	CDE	NLW-10-16E
C5	Capacitor, 75 pf, 5%, N030	RMC	CG75PF
C7	Capacitor, 150 pf, 5%, N150	RMC	CM150PF
C24, 25	Capacitor, 20 pf, 5%	CDE	CM04ED200J03 or CD10ED200J03

REF. DESIGNATION	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NUMBER
RECEIVER P.C. BOARD (A4) (271-225) (Con't)			
C27	Capacitor, 1.2 uf, 25V	Sprague	196D125X9025HA1
C11	Capacitor, 1-18 pf, Var.	Sprague Goodman	GGC-18000
C3	Capacitor, 4.7 uf, 15V	Sprague	150D475X9015B2
C12	Capacitor, 12 pf, 5% Mica	CDE	CM04CD120J03 or CD10CD120J03
C28	Capacitor, 47 uf, 10V	Sprague	150D476X9010R2
C26	Capacitor, 3900 pf	CDE	CD19FD392J03
T1	Transformer	Pulse Engineering or AIE	PE-5762 or 318-0433
K1	Reed Relay	Coto-Coil	1235-12-0101
L1	Tapped Inductor	Bowmar	B6346
L2, 3	Inductor, 100 uh	Lenox-Fugle	NR-100 (LF-100)
L4	Inductor, 330 uh	Lenox-Fugle	NR-330 (LF-330)
TP1 - TP6	Terminal, Turret	Cambion	160-2027-02-01-00
TRANSMITTER P.C. BOARD (A5) (271-226)			
IC11,14,16,18,19	Integrated Circuit TTL		SN7400N
IC13, 20	Integrated Circuit TTL		SN7404N
IC9, 10	Integrated Circuit TTL		SN7420N
IC7, 15, 17	Integrated Circuit TTL		SN7473N
IC1, 4, 12	Integrated Circuit TTL		SN7474N
IC5, 6, 21	Integrated Circuit TTL		SN7493AN
IC2, 3	Integrated Circuit TTL		SN74164N
IC8	Integrated Circuit TTL		SN7486N
Q4,5,6,7,8	Transistor NPN		2N2369A
Q1, 3	Transistor (Not MPS)		2N3904
Q2	Transistor (Not MPS)		2N3906
T1	Pulse Transformer	Pulse Engineering or AIE	PE-5762 318-0433
L1	Coil, 47 uh	Lenox-Fugle	NR47 (LF47)
X1	Crystal, 3.088 MHz	Bowmar	B6221
CR1	Diode		1N4148

REF. DESIGNATION	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NUMBER
TRANSMITTER P.C. BOARD (A5) (271-226) (Con't)			
R10	Resistor, 10K, 1/4W, 5%		RCR07G103JS
R13, 15, 17, 19	Resistor, 6.2K, 1/4W, 5%		RCR07G622JS
R14, 16, 18, 20	Resistor, 360, 1/4W, 5%		RCR07G361JS
R12,33,9,21,34	Resistor, 1K, 1/4W, 5%		RCR07G102JS
R11	Resistor, 4.7K, 1/4W, 5%		RCR07G472JS
R23 - R30	Resistor, 51, 1/4W, 5%		RCR07G510JS
R31, 32	Resistor, 62, 1/4W, 5%		RCR07G620JS
R22	Resistor, 270, 1/4W, 5%		RCR07G271JS
R6	Resistor, 324, 1/8W, 1%		RN60C3240F
R7	Resistor, 357, 1/8W, 1%		RN60C3570F
R8	Resistor, 536, 1/8W, 1%		RN60C5360F
R5	Resistor, 750, 1/8W, 1%		RN60C7500F
R4	Resistor, 1.33K, 1/8W, 1%		RN60C1331F
R3	Resistor, 3.83K, 1/8W, 1%		RN60C3831F
C9	Capacitor, 0.01 uf, 16V	Centralab	UK-16-103
C4,7,8,12,14-19	Capacitor, 0.1 uf, 16V	Centralab	UK-16-104
C10	Capacitor, 220 pf, 5%, Mica	CDE	CM04FD221J03 or CD10FD221J03
C13	Capacitor, 200 pf, 5%, Mica	CDE	CM04FD201J03 or CD10FD201J03
C11, 20, 21	Capacitor, 10 uf, 16V	CDE	NLW-10-16E
C1	Capacitor, 30 pf, N2200, ± 5%	RMC	C30PF
C5, 6	Capacitor, 75 pf, 5%, Mica	CDE	CM04ED750J03 or CD10ED750J03
C3	Capacitor 1-18 pf, Var.	Sprague	GGC-18000
C2 (Selected)	Capacitor, 10 pf, N1500 ± 5% or	RMC or	C10PF
	20 pf, N1500 ± 5% or	RMC or	CG20PF
	30 pf, N1500 ± 5% or	RMC or	CM30PF
	39 pf, N1500 ± 5%	RMC	CM39PF

REF. DESIGNATION	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NUMBER
AUXILIARY P.C. BOARD (A3); 271B-2 Only (271-224)			
R1	Resistor, 30.9K, 1/8W, 1%		RN60C3092F
R2	Resistor, 3.09K, 1/8W, 1%		RN60C3091F
R3, 4	Resistor, 1K, 1/4W, 5%		RCR07G102JS
C1, C2	Capacitor, 4.7 mf, 10%, 15V	Sprague	150D475X9015B2
C3	Capacitor, 10 uf, 16V	Capar or Sprague	CAE-E10M16V or TE-1155E
IC1, 2, 4, 5, 7	Integrated Circuit Hex Inverter		SN7404N
IC3, 6	Integrated Circuit TTL		SN74121N

LIST OF MANUFACTURERS

Abbreviation	Complete Name and Address
AIE	AIE Division of Vernitron 701 Murfreesboro Road Nashville, TN 37210
Beckman	Beckman Instruments Inc. 2500 Harbor Boulevard Fullerton, CA 92634
Bourns	Bourns Inc. 1200 Columbia Avenue Riverside, CA 92507
Bowmar/ALI	Bowmar/ALI, Inc. 531 Main Street Acton, MA 01720
C & K	C & K Components Inc. 15 Riverdale Avenue Newton, MA 02151
Cambion	Cambridge Thermionic Corporation 445 Concord Avenue Cambridge, MA 02138
Capar	Capar 110 Marcus Drive Melville, NY 11747
CDE	Cornell-Dublier Electronics Inc. 150 Avenue "L" Newark, NJ 07105
Centralab	Centralab, Inc. 5757 North Green Bay Avenue Milwaukee, WI 53201
Cinch	TRW/Cinch Connectors 1501 Morse Avenue Elk Grove Village, IL 60007
Coto-Coil	Coto Corporation 65e Pavilion Avenue Providence, RI 02905
Dialco	Dialight 203 Harrison Place Brooklyn, NY 11237

Erie	Erie Technological Products P.O. Box 961 Erie, PA 16512
Fairchild	Fairchild Semiconductor Components 464 Ellis Street Mountain View, CA 94042
G.E.	General Electric Company 1 River Road Schenectady, NY 12345
G.I.	General Instruments Optoelectronics Division 3400 Hillview Avenue Palo Alto, CA 94304
Industrial Devices	Industrial Devices Inc. Edgewater, NJ 07020
Lenox-Fugle	Lenox-Fugle Electronics Inc. 100 Sylvania Place South Plainfield, NJ 07080
Littlefuse	Littlefuse Inc. 800 East Northwest Highway Des Plaines, IL 60016
Lundey	Lundey Associates 51 Newcomb Street Attleboro, MA 02703
Mepco/Electra	Mepco/Electra Inc. 11468 Sorrento Valley Road San Diego, CA 92121
Motorola	Motorola Semiconductor Products Box 20912 Phoenix, AZ 85036
National	National Semiconductor Corporation 2900 Semiconductor Drive Santa Clara, CA 95015
Pulse Engineering	Pulse Engineering Inc. Box 12235 San Diego, CA 92112
RCA	RCA Solid State Division Route 202 Somerville, NJ 08866
RMC	Radio Materials Corporation 4242 West Bryn Mawr Avenue Chicago, IL 60646

Sealectro	Sealectro Corporation 225 Hoyt Street Mamaroneck, NY 10543
Siemens	Siemens Corporation 186 Wood Avenue South Iselin, NJ 08830
Signetics	Signetics Corporation 811 East Arques Avenue Sunnyvale, CA 94086
Silicon General	Silicon General 11651 Monarch Street Garden Grove, CA 92641
Sprague	Sprague Electric Company 481 Marshall Street North Adams, MA 01247
Switchcraft	Switchcraft, Inc. 5555 North Elston Avenue Chicago, IL 60630
T.I.	Texas Instruments, Inc. Box 225012 Dallas, TX 75265
Unitrode	Unitrode Corporation 5 Forbes Road Lexington, MA 02173

www.manualsplus.com
1025790

SE Laboratories
LOC. DD3
MAN – 05615